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PhD in Information and Communication Technologies

On Chip Monitoring for Efficient Thermal Management

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ABSTRACT

Temperature is a critical physical parameter frequently monitored in electronic systems due to its substantial impact on performance and power consumption. In recent years there has been great effort to enhance the technology for development of temperature sensors. Particularly, CMOS-compatible realizations have emerged as a promising alternative, showcasing different physical mechanisms for temperature sensor implementation, including BJTs, Thermal diffusivity and MOSFETs. MOSFET-based temperature sensors offer several advantages, such as low-voltage operation, high energy efficiency, and a compact footprint. Although they may sacrifice resolution and accuracy, this trade-off aligns with the prevalent trend in advanced System-On-Chips designed for Internet-of-Things (IoT) nodes, where these parameters can be relaxed since the priority is energy efficiency while being fully-integrated by handling directly a digital readout, also known as $smart$ temperature sensors. This thesis focus on designing and evaluating energy-efficient $smart$ temperature sensors based on MOSFET devices.

The research encompasses two main achievements. The first involves a $smart$ temperature sensor focused on low-voltage and low-power operation, with a nominal $350\,\mathrm{mV}$ of supply voltage and a power consumption of just $14\,\mathrm{nW}$ at $25\,^{\circ}\mathrm{C}$ with a silicon footprint of $0.049\,\mathrm{mm}^2$, a resolution of $0.27\,^{\circ}\mathrm{C}$ and achieving a Resolution Figure-of-Merit (R-FoM) of $0.034\,\mathrm{nJ{\cdot}K}^2$. This sensor is tailored to meet the stringent constraints of IoT applications.. The second achievement focuses on a compact sensor targeted for Dynamic Thermal Management. The circuit exhibits a wide supply voltage operating range from $0.6\,\mathrm{V}$ to $1.8\,\mathrm{V}$ with an energy per conversion of $1.06\,\mathrm{nJ}$, noise-limited resolution of $0.24\,^{\circ}\mathrm{C}$, a silicon area of $0.021\,\mathrm{mm}^2$, and an a R-FoM of $0.061\,\mathrm{nJ{\cdot}K}^2$. The latter characteristic is particularly notable given the area constraint and the sensor's ability to operate across a broad range of supply voltages.

I. INTRODUCTION

Temperature is one the most frequently measured environmental parameter due to the fact that almost all physical, chemical, mechanical, and biological systems present some form of temperature dependence. The inherent temperature dependence in these systems require precise measurement and control, making temperature monitoring a critical aspect in numerous applications. In the past, temperature sensors were typically constructed using separate components such as resistance temperature detectors (RTDs), thermistors, or thermocouples. However, in recent years, integrated temperature sensors, particularly those leveraging CMOS-compatible designs, have emerged as a promising alternative. Extensive research has been dedicated to the development of compact, cost-effective temperature sensors that integrate readout circuitry, thereby providing temperature measurement in a digital format. These "smart" temperature sensors have now become commonplace. There are several advantages associated with smart sensors [1–8]. Firstly, the generated digital output aligns seamlessly with the demands of modern systems, while avoiding the need for an external analog-to-digital converter (ADC). This increased level of integration reduces the number of components, as well as the size and cost of the sensor. Secondly, in contrast to analog signals, digital signals are less susceptible to interference and they are better suited for accurately transmitting data to other components within a system. Lastly, the integration of the readout circuit and the sensor on the same chip facilitates on-chip digital post-processing, thus simplifying the overall system design.

The temperature-dependent nature of silicon's physical properties open up a range of possibilities for CMOS-compatible devices, including transistors and resistors, that could potentially serve as temperature sensors. However, many of these devices exhibit some shortcomings. Typ-

ically, they produce small analog signals in the millivolt range, further compounded by sensitivity to process variations and packaging-induced stress. The conversion of these signals into digital form is necessary, preferably using a precise on-chip reference, through precision interface electronics. Consequently, the development of accurate CMOS smart temperature sensors represents a considerable challenge [9].

1.1 Motivation

In the era of Internet of Things (IoT), a part of the fourth industrial revolution, the demand for energy-efficient smart temperature sensors has greatly escalated. These sensors play a pivotal role in various applications, including environmental monitoring, industrial automation, healthcare, and smart homes [1, 2, 10, 11]. The reasoning behind the research into energy-efficient smart temperature sensors involve several important aspects:

- Extended Battery Life: Many IoT devices and wireless sensor networks operate on battery power, making energy efficiency a paramount concern. By integrating energy-efficient smart temperature sensors, it becomes possible to prolong the battery life of these devices, thereby reducing the frequency of battery replacements and enhancing their usability and reliability in real-world applications [12].

- Optimized System Performance: Smart temperature sensors serve as critical components in intelligent systems, providing crucial data for temperature monitoring, control, and optimization [2, 13]. By adopting energy-efficient sensor technologies, it becomes feasible to optimize system performance, enhance responsiveness, and achieve higher levels of precision in temperature sensing applications by dynamically adjusting operating voltages and frequencies based on temperature readings [14, 15], thereby improving overall

system efficiency and reliability.

- Miniaturization and Integration: The trend towards miniaturization and integration has fueled the demand for compact and highly integrated sensor solutions. Energy-efficient smart temperature sensors offer the advantage of being compact, lightweight, and easily be integrated within System-On-Chips employed in IoT platforms [13]. This integration enables tighter coupling between temperature sensing and system control, facilitating more efficient thermal management strategies.

- Cost-Effectiveness: Energy-efficient smart temperature sensors not only reduce energy consumption but also contribute to cost savings in terms of battery replacement, maintenance, and operational expenses [9, 13]. By deploying sensors that consume less power, organizations can achieve significant cost reductions over the lifetime of their IoT deployments and sensor networks, making energy efficiency a key consideration in sensor selection and deployment strategies.

The development of energy-efficient smart temperature sensors represents a critical step towards building sustainable, reliable, and intelligent sensing systems for diverse applications. By prioritizing energy efficiency, designers can unlock new possibilities for sensor technology, enabling the creation of innovative solutions that address the evolving needs of the IoT ecosystem and contribute to have more sustainable IoT nodes.

The rest of the thesis is organized as follows. Then CMOS-compatible sensing techniques are discussed in Chapter II and qualitatively compared in Section 2.5. The main works developed during this thesis are presented in Chapters III and IV. Finally, the main outcomes of the proposed designs, conclusions and future work are discussed in Chapter V.

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II. CMOS-COMPATIBLE SENSING TECHNIQUES

As outlined in the introduction, on-chip temperature sensing is widely used in various microelectronics systems, spanning a wide spectrum of application domains [1–17]. Despite the diverse applications, a shared and significant characteristic is evident: they provide temperature information in digital format. This digital output facilitates direct on-chip communication with digital signal processing (DSP) circuits, enabling seamless integration into complex systems. Consequently, they are often referred to as "smart temperature sensors" [18] or Temperature-to-Digital Converters (TDCs).

It is essential to emphasize that the genesis of this category of temperature sensors stemmed from a cost-minimization perspective, and its evolution over the past two decades has predominantly followed this trajectory. While fully integrated temperature sensors in this category may exhibit certain limitations in terms of accuracy and sensing range compared to discrete sensors, their widespread adoption can be attributed to their compatibility with large-scale production of cost-effective products and seamless integration within the host systems. Figure 2.1 shows the conceptual diagram of a smart sensor. It consists of three main components: an Analog Front-End (AFE), an Analog-to-Digital Converter (ADC), and a Digital Back-End (DBE). The input signal to the smart sensor is the temperature itself. The AFE, serving as the initial block in the chain, senses the temperature and converts it into an electrical form, typically in either the voltage or current domain. It generates two crucial signals for Analog-to-Digital conversion: a Proportional-to-Absolute-Temperature (PTAT) signal containing the temperature information, and a reference (REF) signal, ideally exhibiting a Zero-Temperature-Coefficient (ZTC), against which the conversion is conducted.

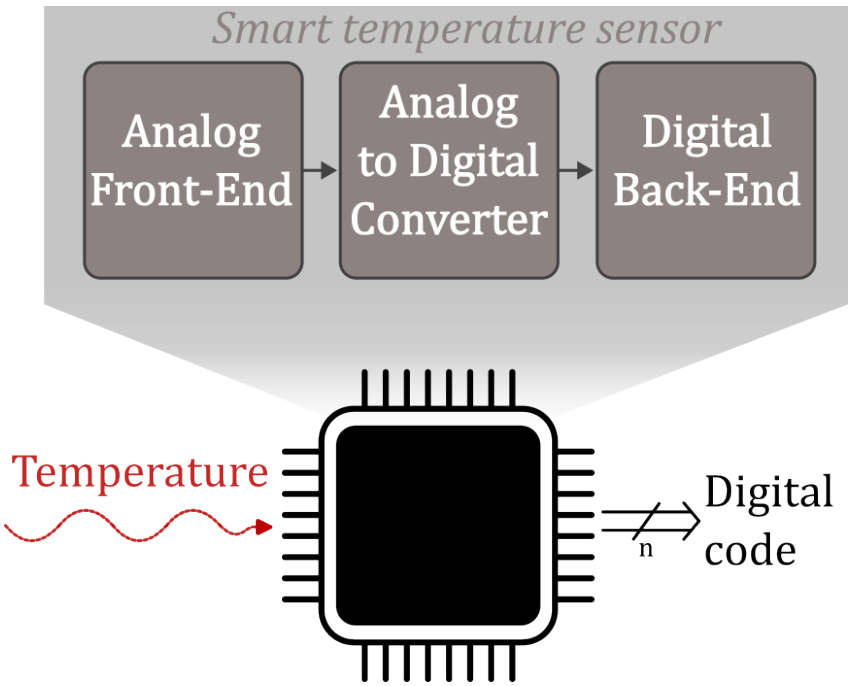

Figure 2.1: Block diagram of an integrated smart temperature sensor

These signals are then fed into the ADC, which produces PTAT digital words with an intrinsic n-bit resolution and a data rate (fS) dependent on the converter architecture. Given the relatively slow variation of the temperature signal compared to the common conversion rates of ADCs, the operation is typically executed without the use of sample and hold (S/H) circuits.

The n-bit codes are subsequently processed by the DBE, acting as an oversampler, to refine their intrinsic resolution through decimation and filtering with a specified Oversampling Ratio (OSR). This process yields output codes from the TDC with higher resolution at the expense of a reduced data rate (f_S/OSR).

In the literature, various ADC architectures have been explored for integration into smart temperature sensors. Examples include $\Sigma\Delta$-based ones [1, 10], SAR-based ones [19, 20], Flash-based temperature sensors [21, 22], hybrid solutions [23, 24] and time/frequency-domain-based ones [25, 26].

The choice of ADC architecture depends on the nature of temperature-dependent signals and specific application requirements. Despite Flash ADCs and SAR ADCs are conceptually faster for a given quantization noise and clock frequency, due to the limitations imposed by thermal noise, the DBE is still in charge of processing the output codes from ADCs. Consequently, for the same level of power consumption, they do not inherently achieve higher energy efficiency compared to $\Sigma\Delta$-based or time/frequency-domain-based alternatives. In practice, $\Sigma\Delta$ converters are often preferred due to their versatility, especially in scenarios where the Analog Front-End generates static temperature-dependent signals. On the other hand, time/frequency-domain-based ADCs are favored for handling dynamic temperature-dependent signals, thanks to their specific characteristics and suitability for such applications.

The DBE effectively enhances the resolution of the output codes while balancing the data rate to meet the requirements of the application.

Thus, the resulting conversion time of a smart sensor can be expressed as:

$$T_{conv} = \frac{1}{f_S \cdot OSR} \tag{1}$$

Given that the smart temperature sensor has a minimum supply voltage V_{DD} and current consumption of I_{DD}, the energy is obtained by:

$$E_{conv} = V_{DD} \cdot I_{DD} \cdot T_{conv} \tag{2}$$

Energy is one of the most important performance parameters of temperature sensors together with the resolution which is defined by various parameters such as the noise (thermal, flicker, ADC quantization, etc) and the conversion time. Usually, resolution can be improved

by increasing the conversion time and, thus, the energy consumption of the sensor. The selected point in the design space will be determined by the specific application requirements of the smart temperature sensor.

Temperature Inaccuracy (T_{Inacc}) is another key parameter of smart temperature sensors. In its absolute form it is defined as the largest temperature error found within the full temperature range of the sensor [27]. From the absolute temperature inaccuracy, the relative form can be extracted by the following relation:

$$T_{Inacc(Rel)} = \frac{T_{Inacc}}{T_{range}} \tag{3}$$

Temperature Inaccuracy is highly dependent of the calibration points selected for a given sensor. The calibration consists in fitting the temperature characteristics of the sensor most commonly by a linear function. Depending on the sensor design, it can be approximated by different calibration methods specified by the trimming points (n_{trim}) used: one point calibration (were the slope is known and quasi constant, of the design), two-point and even three-point. Designers can also directly enhance accuracy by using off-chip non linearity correction techniques, albeit at an increased cost [26, 28–32].

Given the great variety of parameters that can be characterized from a smart temperature sensor, there is the need of defining some Figure of Merits (FoMs) to enable faster comparison between sensors found in the market. These FoMs usually give a specific perspective of the sensor performance. Some of the FoMs are presented in the following [27]:

$$R\text{–}FoM = E_{conv} \cdot (Res)^2 \tag{4}$$

$$T_{Inacc}\text{–}FoM = E_{conv} \cdot (T_{Inacc(Rel)})^2 \tag{5}$$

$$\$\text{–}FoM = (1 + n_{trim}) \cdot \sqrt{\frac{Area}{F^2}} \tag{6}$$

$$Global\text{–}FoM = \frac{E_{conv} \cdot Res \cdot Inacc}{{T_{range}}^2} \cdot (1 + n_{trim}) \cdot \sqrt{\frac{Area}{F^2}} \tag{7}$$

where $Area$ is the silicon space used by the device and F is the feature size of a given technology node. Equations (4) and (5), introduced in [33], present the energy conversion involved with the resolution and the Relative Temperature Inaccuracy, respectively. On the other hand, (6) evaluates the cost production of the sensor by employing the number of trimming points together with the sensor silicon area and the feature size, while (7) gives a general, more global metric, for both performance and cost.

2.1 Resistor based

Resistance temperature detectors (RTDs) have been extensively used as standalone temperature-sensing components. Temperature data is derived by monitoring changes in resistance that are dependent of the temperature. In the realm of CMOS-compatible resistors, most exhibit notable temperature coefficients, ranging between $0.1\%/^\circ\mathrm{C}$ and $0.4\%/^\circ\mathrm{C}$ for 1st-order coefficients. The resistance value can be expressed as:

$$R = R_0(1 + TC \cdot \Delta T) \tag{8}$$

where R_0 is the resistance value at a reference temperature T_0, TC is the corresponding Temperature Coefficient and:

$$\Delta T = T - T_0 \tag{9}$$

A characteristic example is the +0.4%/$^{\circ}\mathrm{C}$ temperature coefficient demonstrated by a typical N-Well or N-Poly resistor, indicating a 72% resistance increase when the temperature spans from -55 $^{\circ}\mathrm{C}$ to 125 $^{\circ}\mathrm{C}$.

In tables 2.1 and 2.2 can be found realistic values for temperature coefficients in 180 and 65 nm technology nodes, respectively[27, 34].

Table 2.1: First order Temperature Coefficients of 180 nm CMOS technology node.

Resistor Type	**TC [K^{-1}]**
n+ diffusion	$+1.5 \cdot 10^{-3}$
p+ diffusion	$+1.5 \cdot 10^{-3}$
n-poly	$-1.5 \cdot 10^{-3}$
n-well	$+3 \cdot 10^{-3}$

Table 2.2: First order Temperature Coefficients of 65 nm CMOS technology node.

Resistor Type	**TC [K^{-1}]**
n+ diffusion with salicide	$+2.2 \cdot 10^{-3}$
n+ diffusion without salicide	$+1.6 \cdot 10^{-3}$
n+ poly with salicide	$+2.2 \cdot 10^{-3}$
n+ poly without salicide	$+1.2 \cdot 10^{-3}$
n-well under oxide diffusion	$+2.5 \cdot 10^{-3}$
n-well under shallow trench isolation	$+2.0 \cdot 10^{-3}$
p+ diffusion with salicide	$+2.4 \cdot 10^{-3}$
p+ diffusion without salicide	$+1.3 \cdot 10^{-3}$
p+ poly with salicide	$+2.4 \cdot 10^{-3}$
p+ poly without salicide	$+3.2 \cdot 10^{-3}$

In resistor-based sensors, the minimum supply voltage is often restricted by the readout circuit, facilitating low supply voltages. The bias current value is dictated by thermal noise and area considerations.[35, 36]

In recent years there has been three main approaches to achieve a temperature conversion to digital code based in the temperature dependence of resistors: Wheatstone bridges, RC filters

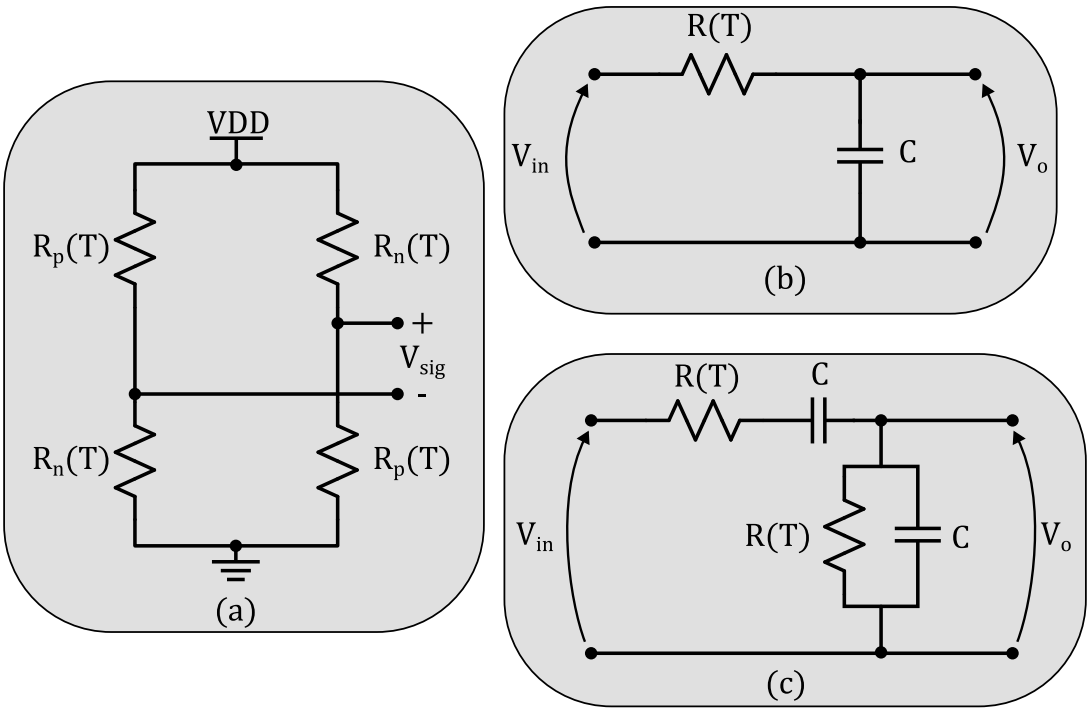

Figure 2.2: Common used circuits to obtain temperature information from integrated resistors. (a) Wheastone bridge, (b) RC filter and (c) Wien-bridge filter.

and Wien-bridge filters. Basic schematics of the general idea are shown in Figure 2.2.

Wheastone bridges-based smart temperature sensors [20, 23, 37–40] usually exploit the effect of two resistors, one with positive temperature coefficient (R_p) and another one with negative temperature coefficient (R_n).

$$R_p = R_0(1 + \alpha\Delta T), \alpha > 0, \tag{10}$$

$$R_n = R_0(1 + \beta\Delta T), \beta < 0, \tag{11}$$

As reported in Figure 2.2, a conversion from temperature change in the resistors to voltage

is read from V_{sig}, which can be expressed as:

$$V_{sig} = \frac{R_p - R_n}{R_p + R_n} \cdot V_{DD} = \frac{R_0(1 + \alpha\Delta T) - R_0(1 + \beta\Delta T)}{R_0(1 + \alpha\Delta T) + R_0(1 + \beta\Delta T)} \cdot V_{DD} = \frac{(\alpha - \beta)\Delta T}{2 + (\alpha + \beta)\Delta T} \cdot V_{DD} \quad (12)$$

In the case of smart temperature sensors based on RC [41–43] and Wien-bridge [34, 44–47] filters the translation is done from temperature to phase shift, as the resistance values change with temperature, the phase response of such filters will change as well. This alteration of the phase response can be sensed by driving the structures with signals oscillating close to the fundamental frequency of the filters [27], the final output is obtained by a phase-to-digital circuit.

A limitation of resistors as temperature-sensing elements lies in the inherent resistance spread in CMOS, typically falling in the 15-20% range across process corners. Moreover, their temperature coefficients are impacted by process variation and higher-order non-linear terms[48, 49]. Consequently, achieving accurate readings with resistors typically necessitates a costly multiple-temperature calibration, with calibration points ranging from 3 to 5 depending on the desired accuracy.

Exemplified by works such as [34] and [44], an accuracy of $\pm 0.15\,^{\circ}\mathrm{C}$ (3σ) from -55 $^{\circ}\mathrm{C}$ to 85 $^{\circ}\mathrm{C}$ is achieved, albeit after an expensive three-temperature trim. Alternatively, [50] accomplishes an accuracy of $\pm 1\,^{\circ}\mathrm{C}$ (3σ) from -45 $^{\circ}\mathrm{C}$ to 125 $^{\circ}\mathrm{C}$ with a single-temperature trim, representing one of the superior results reported for similarly-trimmed resistor-based sensors.

Smart temperature sensors exploiting the above resistor-based temperature conversion techniques are very energy efficient, but offer less accuracy than BJT counterparts and exhibit more power consumption than MOSFET-based architectures.

2.2 BJT based

On-chip temperature sensing can be effectively realized by leveraging the thermal characteristics of the base-to-emitter voltage (VBE) of bipolar transistors when operated in the forward-active region [1, 3, 5, 8, 11, 21, 51–54]. This phenomenon can be mathematically expressed as:

$$V_{BE} = \frac{kT}{q} ln \left(\frac{I_C}{I_S} \right) \tag{13}$$

where k corresponds to the Boltzmann constant, T is the absolute temperature, q is the electron elemental charge, I_C is the BJT collector current and I_S is the saturation current which has a very high sensitivity with respect of the temperature. Equation (13) provides a Complementary-to-absolute Temperature (CTAT) dependence of about -2 $\mathrm{mV/K}$. As a basic example, a Proportional-to-absolute Temperature dependence can be obtained by a pair of BJTs by either having different sizing or supplied with different collector current I_C (Please refer to Figure 2.3), then, the PTAT behaviour is exhibited in the difference of their base-to-emitter voltages:

$$\Delta V_{BE} = \frac{kT}{q} ln \left(a \cdot b \right) \tag{14}$$

where a and b correspond to the ratio of the emitter areas and collector currents, respectively.

The well-defined temperature dependency of the base-to-emitter voltage (V_{BE}) and its variation (ΔV_{BE}) make BJTs appealing for utilization in CMOS temperature sensors and bandgap voltage references. In fact, BJT-based temperature sensors have enjoyed widespread adoption in the industry for decades [19, 55–59]. Several factors contribute to the popularity of BJT-based sensors:

1. Process Inaccuracy Correction: The primary source of inaccuracy in BJT-based sensors

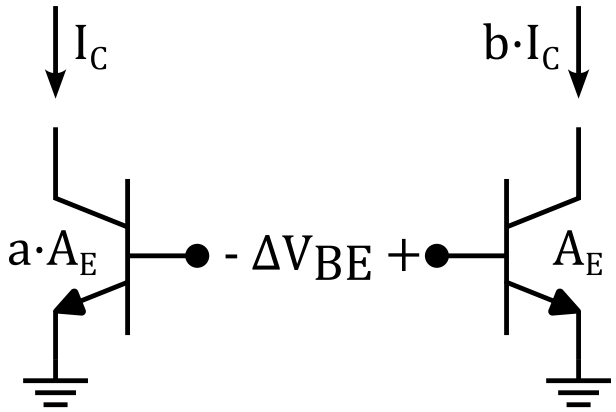

Figure 2.3: BJT pair to generate ΔV_{BE}

stems from the process spread in VBE, which exhibits a PTAT profile [60]. This characteristic allows for cost-effective correction using a one-point PTAT trim. For instance, inaccuracies of $\pm$0.5 °C (3σ) from -50 °C to 120 °C have been achieved [61], and $\pm$0.1 °C (3σ) from -55 °C to 125 °C reported in [62].

2. Single-Circuit Generation of Temperature-Dependent and Reference Voltages: BJT-based sensors generate both the necessary temperature-dependent and reference voltages from the same circuit, significantly simplifying implementation and reducing system complexity.

3. Low Bias Current Requirement: BJT-based sensors operate efficiently with bias currents in the range of microamps (μA) or even sub-microamps (sub-μA), contributing to their energy efficiency.

4. Low Supply Dependency: These sensors typically exhibit low supply dependency, often in the range of a few tenths of degrees Celsius per Volt (°C/V), such as 0.5 °C/V [61] and 0.1 °C/V [62].

These advantages collectively make BJT-based temperature sensors an attractive choice for various applications.

2.3 Thermal Diffusivity based

Thermal diffusivity (D), defined as the rate of which heat diffuses within a silicon substrate, is another category of sensing elements within smart temperature sensors [63–68]. It exhibits relatively high temperature dependence and, more important, it does not suffer from the usual process variation that most devices are subject to. The temperature dependence that D experiences can be approximated by: $D \propto 1/T^{1.8}$ [69–71], due to the well known thermal characteristic of the silicon substrate it is appealing as a core of a smart temperature sensor. To

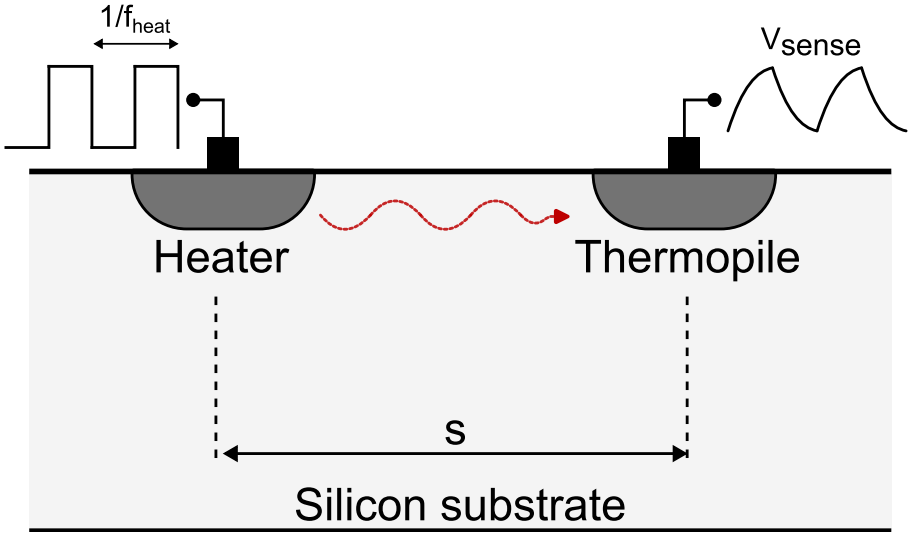

Figure 2.4: Representation of an Electro-Thermal Filter (ETF) in the silicon substrate.

measure D, an Electro-Thermal Filter (ETF) is employed, it is composed by two elements, a heater and a thermopile (Refer to Figure 2.4), the heater is fed by a square wave voltage signal (at frequency f_{heat}) that produces heat accordingly. The heat is then transmitted through the silicon until it is arrived to the thermopile, generating a voltage pulse as a response. The sensed pulse (V_{sense}) by the thermopile is affected by a certain delay characterized by the time needed by the produced heat to traverse the silicon. This delay is a function of the temperature and the phase shift between the voltage pulse at the heater and the sensed pulse at the thermopile can

be represented by [68]:

$$\phi_{EFT} = -s \cdot \sqrt{\frac{f_{heat}}{2D(T)}} \tag{15}$$

A phase-shift ADC can be used to convert the phase shift into a digital code, finalizing the temperature conversion to digital.

A major disadvantage of thermal diffusivity based smart temperature sensors is the inherent high power consumption mainly drawn by the heater making it mostly unsuitable for battery-powered devices[27]. On the other hand, due to the known thermal transfer characteristics these type of sensors usually achieve good accuracy with no trimming [72, 73], this characteristic position them as important competitors in the case of applications when there is no power consumption constraint leading to lowering the cost in mass production since temperature trimming is not necessary to maintain good performance level.

2.4 MOSFET based

MOSFET-based smart temperature sensors can be classified in three categories according to the principle on which they are based for temperature conversion [74]: Type I: Logic, Saturation and Linear, Type II: Subthreshold operation and Type III: Gate leakage. All types will be briefly explained in the following.

2.4.1 Type I: Logic, Saturation and Linear

A typical approach for leveraging MOSFET temperature dependence involves considering the propagation time (t_p) of CMOS inverters (Figure 2.5). t_p is a function of many variables such as supply voltage (V_{DD}), sizing (width (W) and length (L)), carrier mobility (μ), threshold

voltage (V_{th}), oxide capacitance (C_{ox}) and load capacitance (C_L):

$$t_p = f(V_{DD}, V_{th}, W, L, \mu, C_{ox}, C_L) \tag{16}$$

More specifically, both threshold voltage and mobility have their own temperature dependence, providing additional parameters that can be potentially exploited as temperature sensing mechanisms. However, they are affected by doping and lithography variations [74], which also affect the oxide capacitance and the sizing of the transistors.

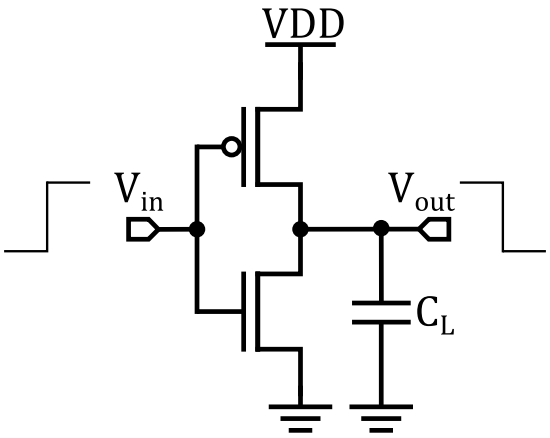

Figure 2.5: A typical CMOS inverter structure

A technique to obtain a temperature reading based on the t_p variation with temperature involves the use of delay lines [23, 75–78]. In reference [75], the temperature-dependent delay is quantized using a phase-locked loop (PLL) implemented on chip. In contrast, works [76, 78] use a temperature-independent delay line for quantization purposes. In [23], the delay line is arranged in a closed-loop configuration to form a ring oscillator, in that way the frequency of oscillation increases with temperature. This temperature-dependent frequency is then quantized using a counter circuit. Each of these approaches offers unique advantages and trade-offs, serving to specific requirements and design considerations for a given temperature sensing

application.

For the case of smart temperature sensors based on MOS devices working in saturation region [79], the thermal coefficient and operating principle is similar to that of t_p based. The saturation current can be expressed as [80]:

$$I_{sat} = \frac{1}{2}\mu C_{ox}\left(\frac{W}{L}\right)(V_{gs} - V_{th})^2(1 + \lambda V_{ds}) \tag{17}$$

where V_{gs} and V_{ds} are the gate-source and drain-source voltages, respectively. The current described by Equation (17) can be effectively used to regulate a delay line, as illustrated in Figure 2.6, where V_{BIASN} corresponds directly to V_{gs} in (17), while $VDD - V_{BIASP}$ act as V_{sg} for the PMOS head transistor. The delay line can be regulated by both head and tail transistors driven by V_{BIASP} and V_{BIASN}, or by a single transistor either head or tail. Specifically,

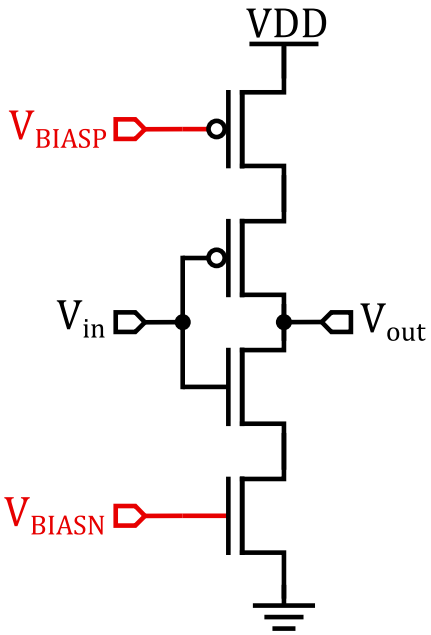

Figure 2.6: A current-starved CMOS inverter

adjusting the V_{gs} voltage can lead to changes in the I_{sat} thermal coefficient from negative to

positive. This phenomenon occurs because both μ and V_{th} possess negative thermal coefficients in Equation (17). However, as V_{gs} diminishes, the contribution of $(V_{gs} - V_{th})$'s positive thermal coefficient intensifies, counteracting the negative coefficient from μ, and consequently changing the overall thermal coefficient sign. Essentially, as V_{gs} decreases, the thermal coefficient for the current-starved cell delay shifts from positive to negative, given that the discharge time corresponds to $t_{\text{dis}} = C_L \cdot V_{\text{DD}}/I_{\text{dis}}$.

Moreover, the thermal coefficient of the entire delay line may approach zero when V_{DD} is approximately $0.75V$ for a 55-nm technology node [74]. This ZTC point is crucial and serves as the foundation for the temperature-insensitive reference delay line discussed in previous literature [23, 77, 81]. Similarly, the same zero temperature coefficient may be attained for the current-starved delay line, such as when $V_{BIASN} = 0.75V$ in Figure 2.6. This ZTC point is crucial for achieving temperature-insensitive operation, ensuring the robustness and reliability of the delay line across temperature variations.

In [29], temperature estimation is derived from the comparison of oscillation frequencies between two voltage-controlled ring oscillators with distinct V_{th} values. This approach effectively mitigates the supply voltage sensitivity compared to a single oscillator alternative. Similarly, the temperature sensor outlined in [22], produces a voltage output instead of a delay. Additionally, the temperature-dependent delay can be quantized by a time-domain $\Delta\Sigma$ ADC, as demonstrated in [82].

MOSFET devices working in linear region can also be used as temperature sensing element [83]. The drain current of such devices for small V_{ds} can be approximately represented by:

$$I_{lin} \approx \mu C_{ox} \left(\frac{W}{L}\right) (V_{gs} - V_{th}) V_{ds} \tag{18}$$

The thermal behaviour of the linear current expressed in (18) has a typical CTAT response, ruled by μ in the case of large enough V_{gs}. But, as shown in [83], for when V_{gs} is close to 0.7V for a 180- nm technology node the non-linearity of the sensor falls to its minimum value. This CTAT current is then discharged through a capacitor, that has a propagation delay with PTAT behaviour due to the inverse proportion relation between the discharge time and the supplied current. When V_{ds} in (17) is biased based on a proportion from V_{DD} the supply sensitivity of the discharge time t_{dis} is diminished [83].

2.4.2 Type II: Subthreshold operation

A MOSFET device works in subthreshold region when the $V_{gs} < V_{th}$. In this condition, the drain current can be represented by [9, 80]:

$$I_{sub} = \mu C_{ox} \left(\frac{W}{L}\right) {V_T}^2 \exp\left(\frac{V_{gs} - V_{th}}{nV_T}\right) \left[1 - exp\left(\frac{-V_{ds}}{V_T}\right)\right] \tag{19}$$

where V_T is the thermal voltage (kT/q). In the case of $V_{ds} > 3V_T$ the equation (19) reduces to:

$$I_{sub} = \mu C_{ox} \left(\frac{W}{L}\right) {V_T}^2 \exp\left(\frac{V_{gs} - V_{th}}{nV_T}\right) \tag{20}$$

A PTAT voltage can be produced by two MOSFETs M_1 and M_2 while working in subthreshold regime as illustrated in Figure 2.7, their drain current could be expressed as:

$$\mu C_{ox} \left(\frac{W}{L}\right) {V_T}^2 \exp\left(\frac{Vgs,1 - V_{th,1}}{nV_T}\right) = K \cdot \mu C_{ox} \left(\frac{mW}{L}\right) {V_T}^2 \exp\left(\frac{Vgs,2 - V_{th,2}}{nV_T}\right) \tag{21}$$

Thus, a differential voltage from their gates/drains to source ΔV_{gs} can be obtained:

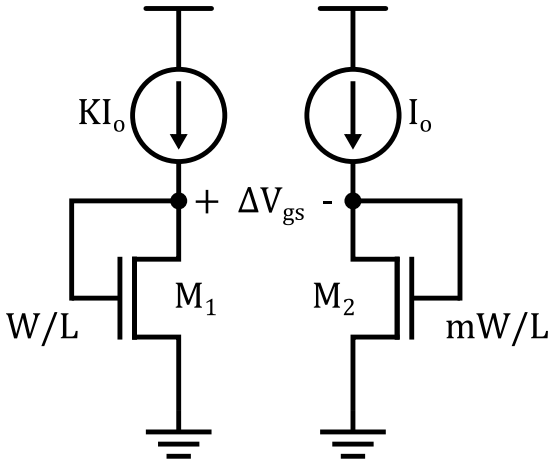

Figure 2.7: PTAT voltage generation from a pair of MOSFET devices in subthreshold regime.

$$\Delta V_{gs} = V_{gs,1} - V_{gs,2} = nV_T \ln(m \cdot K) \tag{22}$$

where $m \cdot K > 1$ and $V_{th1} = V_{th2}$ (no mismatch between devices). Equation (2.7) is analogous to what is achievable with BJTs counterparts (Figure 2.3 and Equation (14)). Works presented in [9, 84, 85] base their proposals in PTAT voltages converted into PTAT currents via a resistor with low thermal coefficient. In [9], the use of a capacitor enabled a conversion from the PTAT current to a CTAT delay with $t_{dis} = C_L \cdot V_{DD}/I_{dis}$. While in [84] a CTAT oscillation frequency was obtained after feeding the PTAT current into a ring oscillator, finally, a digital output is obtained by quantizing the oscillation frequency with a counter. Other works utilize subthreshold currents to feed ring oscillators. In order to remove the need of a reference frequency, two currents can be employed with two current-starving ring oscillators and the digital code is obtained after quantizing the ratio of the resulting oscillation frequencies [26, 86–88]. The key aspect is that the control of the oscillators is done by proportional currents or devices with different threshold voltages. The use of $\Delta\Sigma$ ADCs to quantize a PTAT voltage analogous to the described in (22) allowed to obtain better accuracy and resolution in the case of works [89, 90], while for [91] it assisted in obtaining a wider temperature range.

2.4.3 Type III: Gate leakage

A gate leakage-based temperature sensor was introduced at CICC 2019[92]. This sensor integrated a MOSFET between the power supply and the current-starved ring oscillator. The MOSFET gate was directly connected to the power supply, while its drain, source, and body were short circuited and linked to the ring oscillator's supply node, as shown Figure 2.8. Consequently, the gate leakage current of the MOSFET regulated the oscillation frequency of the ring oscillator.

One notable advantage of the gate leakage-based temperature sensor proposed in [92] was its exceptional energy efficiency, surpassing the state-of-the-art works at the time of publication by a factor of seven. This efficiency stemmed from its sensing front-end, which relied on the gate leakage current and consumed merely 640pW. Another work utilizing gate-leakage current levels in a temperature sensor is reference [93], where both thermal-dependent gate-leakage current and subthreshold MOSFETs are employed to generate a current reference in pA levels.

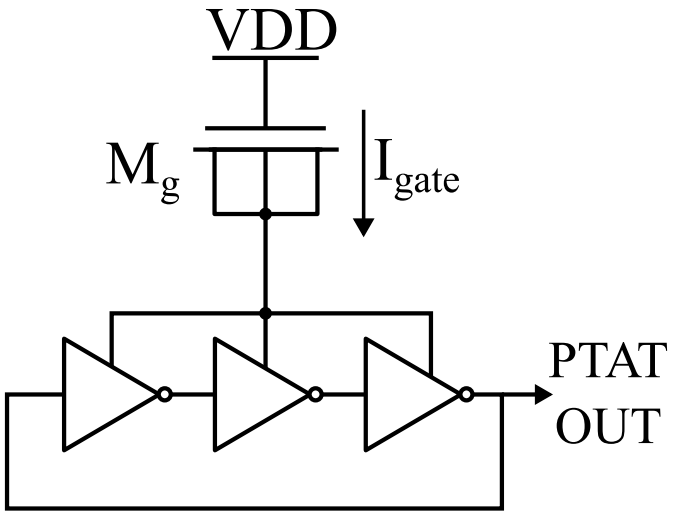

Figure 2.8: Ring oscillator for PTAT frequency generation biased by a gate-leakage current featured by transistor M_g [92].

2.5 Qualitative comparison

Each of the discussed sensing mechanisms has its own trade-off. Thermal diffusivity-based sensors, for example, stand out in terms of required calibration points and accuracy. They can achieve high accuracy with no trimming but -occasionally- just batch calibration, due to the use of the thermal characteristics from the material itself effectively diminishing the process variability impact on the temperature sensing solution. BJT-based sensors achieve high precision due to their well-defined thermal characteristics. Moreover,in some cases the use of 1-point calibration is enough for this class of sensors. MOSFET solutions on the other hand usually require about 2 points for temperature calibration, although the number of required points depends on several factors such as production cost and demanded accuracy of the target application. Smart sensors based on resistors are more limited in this regard, as the resistance spread after the effects of process variability is rather high, thus, to achieve competitive values of inaccuracy the use of multi-point calibration is necessary.

Albeit the disadvantage of resistor-based smart temperature sensors in accuracy, the energy per conversion (required energy to perform one full temperature-to-digital conversion) this solution offers is the best among the reviewed mechanisms, BJT- and MOSFET-based sensors achieve similar levels of consumed energy per conversion with no clear advantage one over the other. Finally, smart temperature sensors based on the thermal diffusivity principle exhibit the least appealing efficiency due to the required energy produced by the heater, making them unsuitable for battery powered applications such as IoT. Taking into account the Resolution-FoM (R-FoM) presented in (4) which uses the resolution of the sensor by a square factor, the energy efficiency of the sensor can be characterized, this efficiency can be defined as the energy cost to achieve a certain resolution. Due to the low energy consumption per conversion and the high

accuracy they offer, resistor-based temperature sensors present a highly competitive R-FoM within this sensing mechanism category. They are closely followed by sensors relying on BJT and MOSFET. The latter two types typically exhibit similar levels of energy efficiency, with MOSFET-based sensors holding a slight advantage. In contrast, thermal diffusivity-based sensors demonstrate the lowest R-FoM due to the intrinsic high power requirements for operation.

Smart temperature sensors employing MOSFET devices offer distinct advantages, particularly in Type II configurations (Section 2.4.2), where subthreshold thermal characteristics are exploited for temperature conversion. Notably, they facilitate low voltage operation, thus enhancing energy efficiency. Furthermore, MOSFET-based sensors exhibit a compact footprint, optimizing silicon area utilization [27]. On the other hand, thermal diffusivity-based sensors, while occupying a similar silicon area, exhibit inferior voltage scaling capabilities [94]. BJT counterparts, although competitive, have poor supply voltage scaling as well, while maintaining a moderate silicon footprint, comparable to resistor-based sensors. These observations stress MOSFET-based sensors as a compelling choice for smart temperature sensing applications with constraints in silicon area occupancy, voltage scaling and energy efficiency, trading off these characteristics with performance in terms of accuracy.

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III. PROPOSED DESIGN: AN ULTRA-LOW VOLTAGE, ULTRA-LOW POWER, ENERGY-EFFICIENT SMART TEMPERATURE SENSOR

3.1 Introduction

In recent times, there has been a widespread use of portable, battery-operated devices that have the capability to detect the surrounding environment and transmit the obtained information wirelessly, after some form of data manipulation, recognition, and/or classification. These devices, collectively known as the Internet of Things (IoT), all share a common requirement for limited power consumption (e.g., in the range of a few milliwatts) [1]. To achieve energy efficiency approaching the bare minimum, IoT devices can be designed with scaled-down supply voltages, sometimes reaching levels close to or below the sub-threshold voltage [2–4]. Furthermore, there is an increasing demand for reducing the size of the integrated circuit, as this is seen as a highly desirable attribute for enabling cost-effective system integration.

Temperature sensors play a crucial role in various applications, including thermal regulation and management of processors or systems on chip (SoCs) [5–8], monitoring ambient temperature [9], and in biomedical devices [10, 11]. Moreover, their use is notable in IoT devices [12–17], where a trade-off between achieving a few nW of power consumption for effective extension of battery life and a moderate resolution of a few $^{\circ}\mathrm{C}$ is often considered.

Diverse mechanisms for temperature sensing are outlined in [18]. In a Complementary

Metal-Oxide-Semiconductor (CMOS) process, the most established method involves exploiting the temperature-dependent characteristics of the built-in voltages in parasitic Bipolar Junction Transistors (BJT) [6, 14]. An Analog-to-Digital Converter (ADC) is then employed to acquire a digital representation of the temperature, facilitating the attainment of temperature accuracy of less than ± 0.1 °C across a broad temperature range (from 55 °C to 125 °C) with only one-point calibration [19]. However, this approach mandates substantial supply voltages (typically exceeding 1 V) and consumes micro-watts of power [14]. Resistors offer a potential alternative to BJT-based sensors, albeit with the caveat that the sensing elements tend to occupy a significantly larger area [20].

As shown in [15], temperature sensors employing MOSFET devices exhibit the potential for superior energy efficiency compared to the previously mentioned solutions, albeit at the expense of reduced accuracy and more intricate calibration procedures. This category of circuits commonly employs MOSFETs operating in the sub-threshold region as sensing components, facilitating the development of compact temperature sensing designs characterized by a power supply voltage of less than 1 V and power consumption of 1 μW or lower [12–15, 21]. These designs find significant relevance in various practical IoT applications, where there exists flexibility in the requirements for accuracy and resolution.

The proposed temperature sensor operates at an exceptionally low voltage of 0.35 V, rendering it particularly suitable for applications within the constrained energy resources of the Internet of Things. Temperature measure is facilitated by a sensing circuit employing PMOS devices. This circuit transforms temperature variations into two biasing sub-threshold currents to establish two oscillation frequencies. With an increase in temperature, these frequencies exhibit a linearly escalating ratio. Subsequently, the obtained frequency ratio undergoes con-

version into a digital output code through a digital backend composed by binary counters.

The sensor is fabricated using 180-nm CMOS technology and occupies a modest silicon area of less than $0.05\,\mathrm{mm}^2$. When energized at $350\,\mathrm{mV}$, the circuit's power consumption is a mere $14\,\mathrm{nW}$ at a temperature of $25\,^{\circ}\mathrm{C}$. Additionally, the energy for each conversion stands at a minimal $0.46\,\mathrm{nJ}$, while maintaining an acceptable level of inaccuracy within the range of $\pm 3\,^{\circ}\mathrm{C}$, characterized by a typical root mean square inaccuracy of $1.2\,^{\circ}\mathrm{C}$. Furthermore, it provides a resolution lower than $0.3\,^{\circ}\mathrm{C}$ within the temperature span of $0\,^{\circ}\mathrm{C}$ to $100\,^{\circ}\mathrm{C}$.

3.2 Sensor architecture and operating principle

As depicted in Figure 3.1, our design consists of three main sub-circuits: 1) a Temperature-to-Current Converter (TCC), 2) a Current-to-Frequency Converter (CFC), and 3) a Frequency-to-Digital Converter (FDC). The TCC operates by detecting the real temperature and simultaneously producing two sub-threshold currents (I_L, I_H). The relationship between these currents, I_H/I_L, demonstrates a behavior that is directly proportional to absolute temperature (PTAT) within the specified temperature range of $0\,^{\circ}\mathrm{C}$ to $100\,^{\circ}\mathrm{C}$. Afterwards, these currents undergo a linear transformation into two frequencies (f_H, f_L) by utilizing two current-starved differential ring oscillators that implement the CFC mechanism. Finally, the FDC generates the digital output code (DPTAT), which is derived from the frequency ratio f_H/f_L.

3.2.1 Temperature to Current Converter

The employed temperature sensing methodology involves a key aspect that centers around the generation of two currents, I_H and I_L, which are characterized by a linear PTAT behavior within the designated temperature range. The reliable generation of these currents is achieved

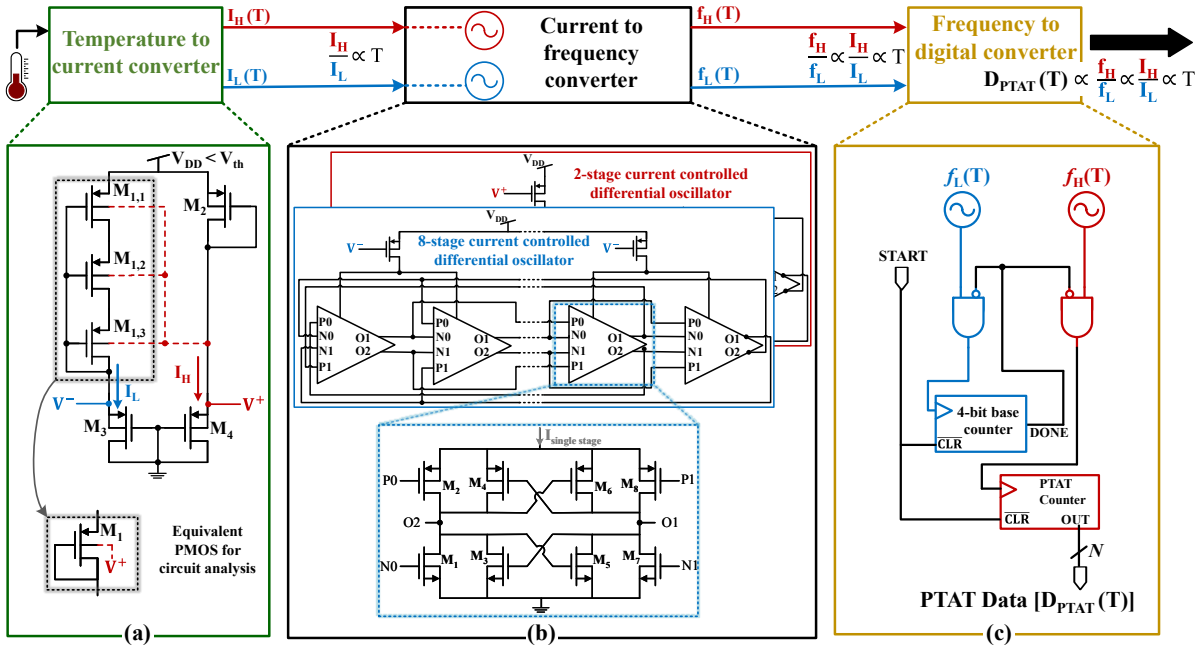

Figure 3.1: Block diagram of the temperature-to-digital converter: (a) the temperature-to-current converter (TCC), (b) the current-to-frequency converter (CFC) and (c) the frequency-to-digital converter (FDC).

through the utilization of a two-branch TCC depicted in Figure 3.1, where PMOS diodes connected in series establish sub-threshold currents with the desired IH/IL ratio. Only PMOS devices where used in this structure to mitigate process variations by utilizing devices of the same type. To better explain the circuit behaviour, the TCC can be simplified by combining the stacked transistors $M_{1,1}$ to $M_{1,3}$ into an equivalent device denoted as M_1. It is important to note that all PMOS transistors in the TCC operate in the sub-threshold region and have a source-to-drain voltage, VSD, that exceeds four thermal voltages $V_T = k_B T/q$. Here, k_B represents the Boltzmann constant, T represents the absolute temperature, and q represents the electron charge. The source current I_S can be mathematically expressed as [22]:

$$I_S = \frac{W}{L} I_0 \, exp\left(\frac{q(|V_{GS}| - |V_{th}|}{nk_B T}\right) \tag{23}$$

where V_{th} is the threshold voltage, I_0 is the technology-dependent sub-threshold current extrapolated for $|V_{GS}|$=$|V_{th}|$, W/L is the aspect ratio of the transistor and n is the sub-threshold factor. In (23), the V_{th} has a dependency on V_{SD} (through the drain induced barrier lowering (DIBL) effect) and on the source-to-bulk voltage V_{SB} (through the body effect) [22]. The expression of the V^+ – V^- voltage can be derived by analyzing the upper segment of the TCC circuit:

$$V^+ - V^- = \Delta V_{th} + \frac{nk_BT}{q} \ln\left(\frac{I_L/\left[\frac{W}{L}\right]_1}{I_H/\left[\frac{W}{L}\right]_2}\right) \tag{24}$$

where ΔV_{th} = $|V_{th1}|$ – $|V_{th2}|$. In the case where M_3 and M_4 possess identical characteristics, specifically with respect to their W/L ratios and threshold voltages, the voltage difference between V^+ and V^- can be alternatively represented as a function of the currents passing through M_3 and M_4:

$$V^+ - V^- = \frac{nk_BT}{q} \ln\left(\frac{I_H}{I_L}\right) \tag{25}$$

Finally, the final current ratio I_H/I_L expression can be obtained by equating (24) and (25):

$$\Delta V_{th} + \frac{nk_BT}{q} \ln\left(\frac{I_L/\left[\frac{W}{L}\right]_1}{I_H/\left[\frac{W}{L}\right]_2}\right) = \frac{nk_BT}{q} \ln\left(\frac{I_H}{I_L}\right) \tag{26}$$

$$\Delta V_{th} = \frac{nk_BT}{q} \ln\left(\frac{I_H}{I_L} \cdot \frac{I_H/\left[\frac{W}{L}\right]_2}{I_L/\left[\frac{W}{L}\right]_1}\right) \tag{27}$$

$$\frac{q\Delta V_{th}}{nk_BT} = \ln\left(\left(\frac{I_H}{I_L}\right)^2 \frac{\left[\frac{W}{L}\right]_1}{\left[\frac{W}{L}\right]_2}\right) \tag{28}$$

$$\frac{I_H}{I_L} = \sqrt{\frac{\left[\frac{W}{L}\right]_2}{\left[\frac{W}{L}\right]_1}}\, exp\left(\frac{\Delta V_{th} q}{2nk_B} \cdot \frac{1}{T}\right). \tag{29}$$

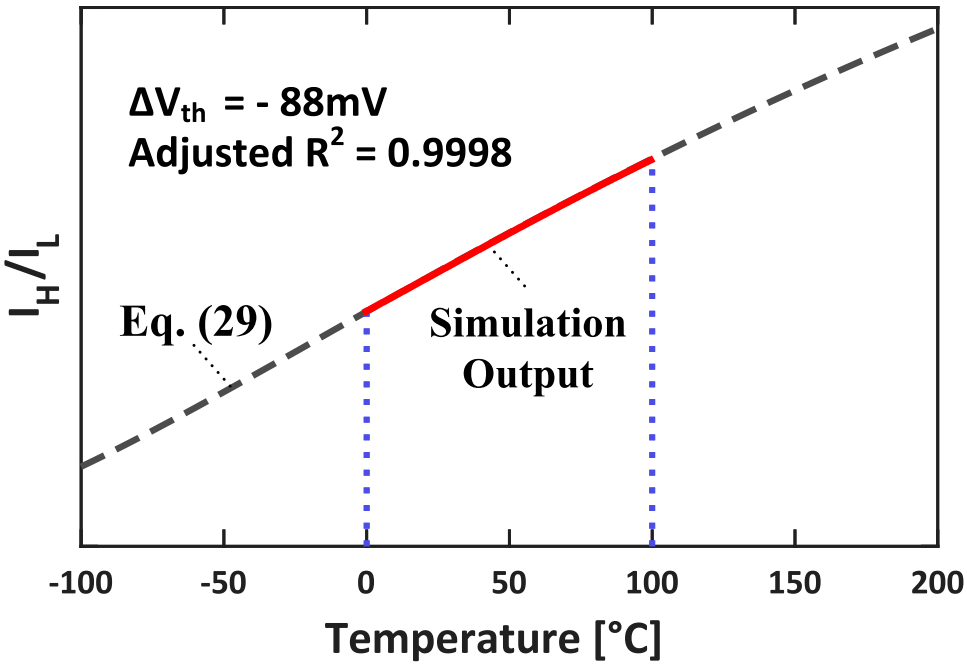

Figure 3.2: Temperature-sensing mechanism.

It is important to highlight that in (29), the change in threshold voltage, ΔV_{th}, remains constant regardless of temperature, even though $|V_{th1}|$ and $|V_{th2}|$ exhibit both CTAT and linear characteristics in the target temperature range. When $|\Delta V_{th}|$ exceeds $70\,\mathrm{mV}$, equation (29) can be effectively approximated by its linearization. This is shown in Figure 3.2 for $|\Delta V_{th}|$= $88\,\mathrm{mV}$. To achieve this specified value, connecting the body terminal of the stacked transistors $\mathrm{M}_{1,1}$ to $\mathrm{M}_{1,3}$ to the V^+ node is essential. This configuration facilitates in obtaining the desired ΔV_{th} while exclusively utilizing PMOS devices. As depicted in Figure 3.2, the adjusted R^2 [14], for the simulated ratio of high-current (I_H) to low-current (I_L) exhibits a noteworthy magnitude of 0.9998 when considering the temperature span from $0\,^{\circ}\mathrm{C}$ to $100\,^{\circ}\mathrm{C}$. This elevated R^2 value serves to confirm the crucial characteristic of linearity in the response of the implemented TCC circuit.

3.2.2 Current to Frequency Converter

As illustrated in Figure 3.1(b), the CFC is composed of a pair of current-controlled differential oscillators employing two and eight stages, respectively. These oscillators are biased by a mirrored version of the currents I_H and I_L, with I_H and I_L being the high and low currents, respectively. Furthermore, the oscillation frequency is denoted as f_H and f_L, where $f_H > f_L$. The differential delay cell is inherited from the design presented in [23].

The inputs of the delay cell are connected to both NMOS transistors (M_1, M_7) and PMOS transistors (M_2, M_8). To minimize the influence of rising/falling slopes on the oscillation frequency, the NMOS inputs receive signals from the outputs of the preceding delay stage, while those of the PMOS devices are sourced from the outputs of an even earlier delay stage, as suggested by prior work [23]. Subsequently, the NMOS/PMOS pairs (M_3, M_5)/(M_4, M_6) configured in a cross-coupled manner speed-up the restoration of logic levels at the output of the inverters, thus, accelerating the switching stage [23].

By adopting this configuration, the oscillation frequency becomes almost linear with the sub-threshold current of the oscillator, denoted as I_{bias}. This linearity can be effectively approximated using the following expression [23]:

$$f_{osc} = \frac{1}{2N\tau} = \frac{I_{bias}}{2NC_LV} \tag{30}$$

where N is the number of the delay stages, τ is the delay time in a single stage, V is the oscillation amplitude, and C_L is the load capacitance. The two differential oscillators have been carefully designed, incorporating an optimal number of stages and appropriately sized delay stages. This design strategy contributes to an overall enhancement of the resolution in

the f_H/f_L ratio.

3.2.3 Frequency to Digital Converter

The frequencies generated, denoted as f_H and f_L, undergo conversion into a digital PTAT output utilizing two asynchronous counters, as depicted in Figure 3.1(c). A 4-bit basic counter is employed to enhance the resolution of the temperature sensor, effectively dividing the f_L frequency by 8. Meanwhile, the PTAT counter, driven by the f_H frequency, comprises 11 bits. The selection of the PTAT counter size is deliberate, ensuring prevention of counting overflow across the temperature detection range from 0 °C to 100 °C, while also accounting for potential undesired offsets arising from process variations.

Upon triggering the $START$ signal, the oscillators initiate their operation, and both counters commence counting upwards. The counters cease operation when the fourth bit of the basic counter transitions to logic 1, signifying the completion of eight cycles of the slower oscillator. This event triggers the $DONE$ signal. At this juncture, the digital code corresponding to the temperature can be retrieved from the PTAT counter. The counters are subsequently reset by the $START$ signal, facilitating a new temperature measurement when required.

3.3 Monte Carlo Analysis

Figure 3.3(a)-(c) present the deviation, or inaccuracy, of the digital output from our sensor compared to the reference calibrated transfer characteristics. These reference characteristics are derived from calibration points at 10 °C and 90 °C. The temperature considered for this analysis is 30 °C. The data are obtained after 1000 Monte Carlo (MC) simulations for three distinct values of V_{DD}: (a) 0.3 V, (b) 0.35 V, and (c) 0.4 V, respectively. Notably, the visual

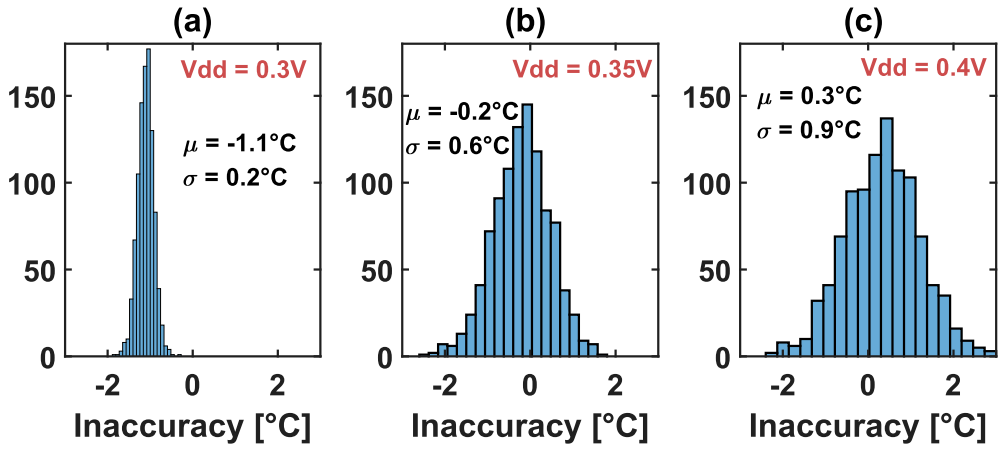

Figure 3.3: Inaccuracy at T = 30 °C, as evaluated by 1000 MC simulations for V_{DD} = (a) 0.3 V, (b) 0.35 V and (c) 0.4 V, respectively.

representation demonstrates that the anticipated inaccuracy falls within an acceptable range of approximately ±3 °C for the reference temperature of 30 °C.

3.4 Measurement Results

The implemented temperature sensor is manufactured using a 180- nm CMOS technology, with a compact footprint with a silicon area of 0.049 μm^2. A visual representation of the chip is shown in Figure 3.4(a), illustrating the die photo. Additionally, Figure 3.4(b) provides the layout of the circuit higlighting each part of the sensor. The temperature sensing core, denoted as TCC, occupies just 4662 μm^2. Meanwhile, the CFC and FDC circuits cover larger areas, occupying 24928 μm^2 and 17029 μm^2, respectively. Measurements were conducted on

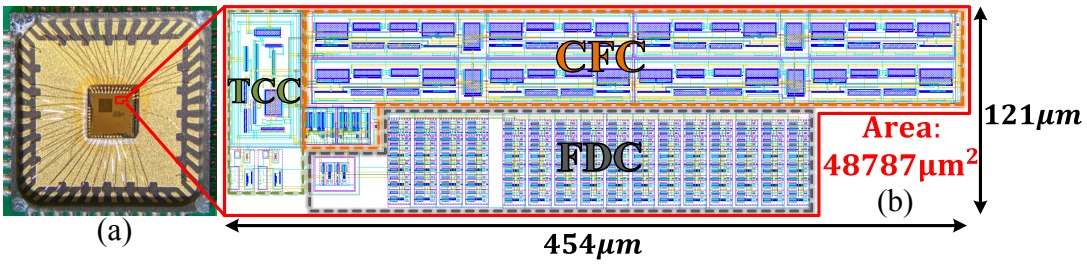

Figure 3.4: Micrograph (a) of the testing chip and layout (b) of the proposed temperature sensor.

9 dies. Specifically, at a supply voltage of V_{DD} = 0.35 V, the frequencies of the two differential oscillators spanned from a few hundred Hz to a few tens of kHz for the slow and fast oscillators, respectively, as the temperature varied between 0 °C and 100 °C. Each sample has been independently calibrated, employing a 2-point calibration scheme using 10 °C and 90 °C as reference temperatures. In Figure 3.5, the digital output generated by each sample is presented as a function of temperature, accompanied by the corresponding calibrated transfer characteristics. This representation highlights the observed linearity, evidenced by an RMS adjusted R^2

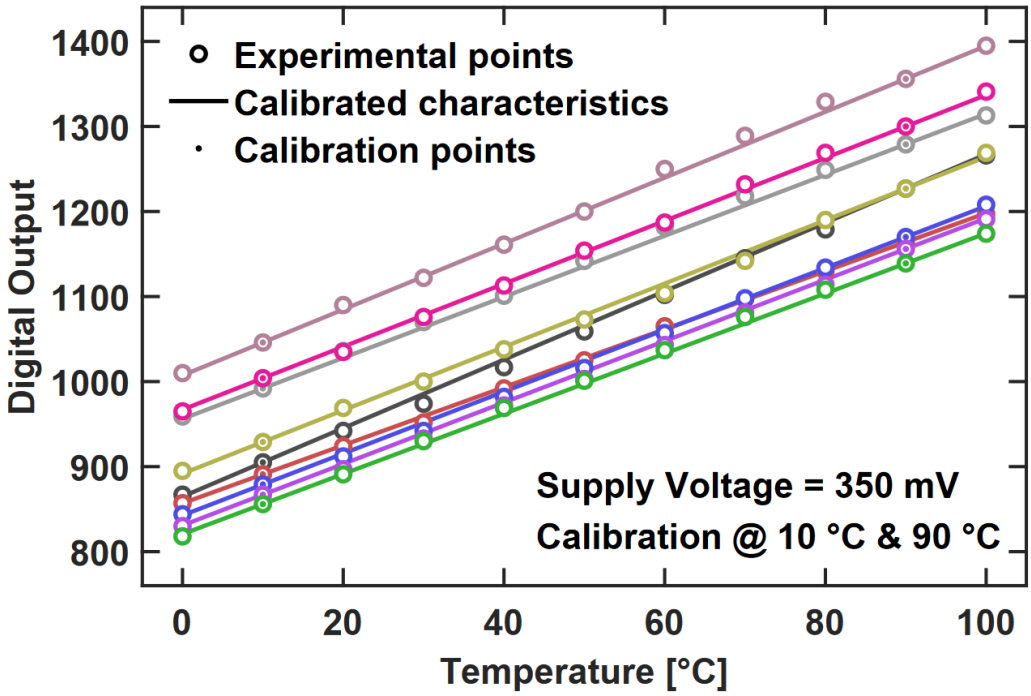

Figure 3.5: Measured digital output extracted after two-point calibration as a function of the temperature in the 0 °C, 100 °C range, V_{DD} = 350 mV.

value equal to 0.9989. It's worth noting that this value is slightly degraded in comparison to the simulation value reported for I_H/I_L in Figure 3.2. In Figure 3.6, the inaccuracy is reported for each sample as a function of the temperature. In Figure 3.7(a-c), die-to-die variability is accounted for, presenting box plots for (a) the digital output produced by each sensor at 30 °C, (b) the sensor resolution (inverse slope of calibrated transfer characteristics), and (c) the inac-

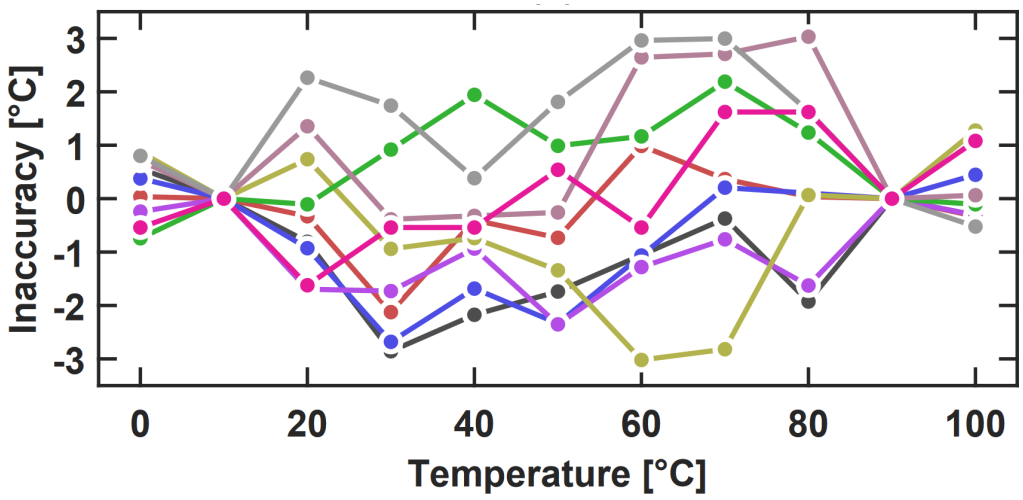

Figure 3.6: Measured Inaccuracy extracted after two-point calibration as a function of the temperature in the 0 °C, 100 °C range, V_{DD} = 350 mV.

curacy, measured in both RMS and peak terms. Considering the die-to-die deviations observed

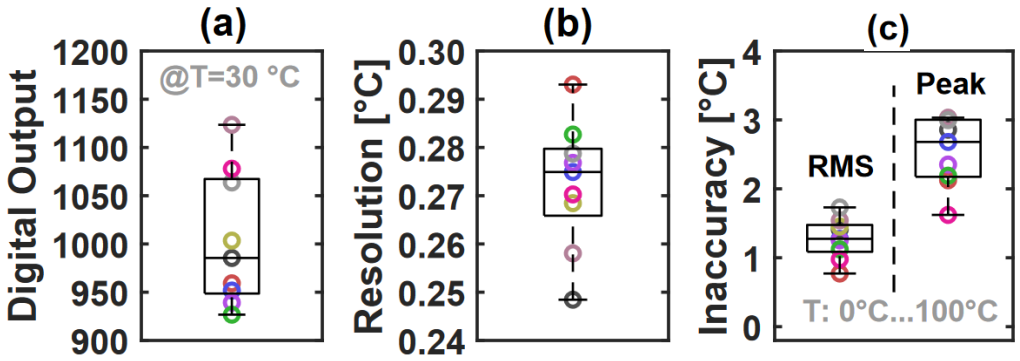

Figure 3.7: Die-to-die variability box plots of (a) digital output at 30 °C, (b) temperature resolution (inverse slope of calibration curves in Figure 3.5) and (c) inaccuracy (RMS and peak errors).

for the 30 °C digital outputs (a) and for the resolutions (b) denoting vertical offset and inverse slope of transfer characteristics, respectively exhibited by different sensors operating under the same conditions, it becomes evident that calibration for each individual device is imperative for our sensor.

For instance, with a median resolution of 0.275 °C, a deviation of 50 in the digital output would translate to an unacceptable inaccuracy exceeding 13 °C. However, post-calibration,

each sensor can capitalize on the high resolution (with the worst-case measured value at 0.295 °C) to achieve a reduced inaccuracy. The median RMS and peak inaccuracies are 1.2 °C and 3.1 °C,

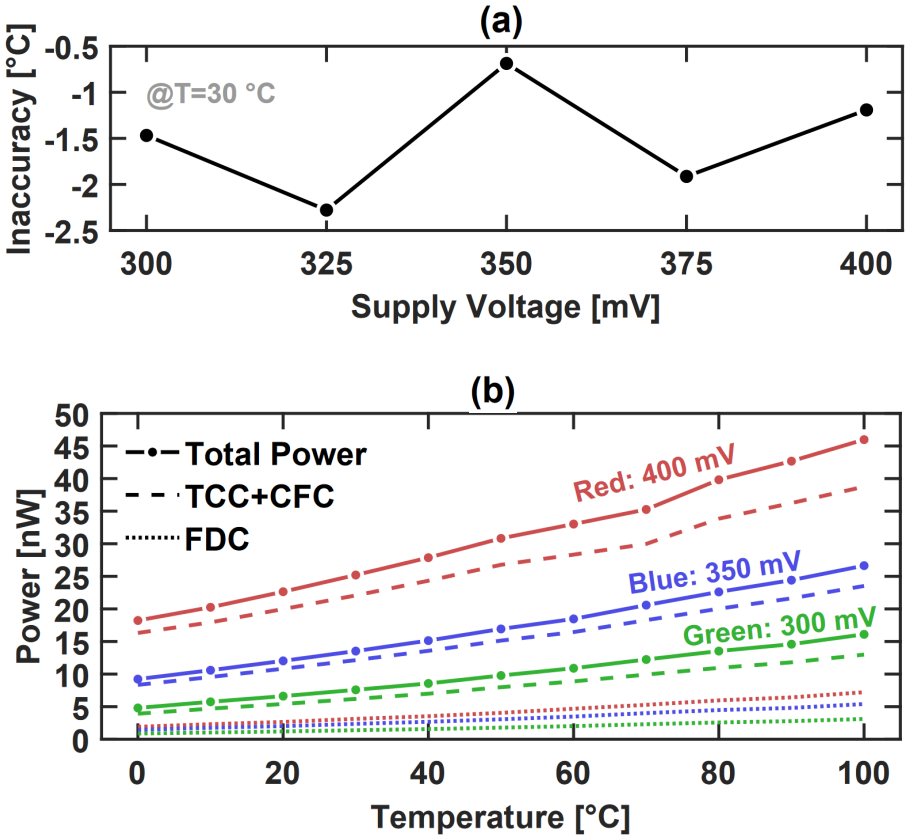

Figure 3.8: Measured (a) line sensitivity at 30 °C as a function of the supply voltage and (b) power consumption of temperature-to-current converter (TCC), current-to-frequency converter (CFC) and frequency-to-digital converter (FDC) as a function of temperature. (a) and (b) are extracted on a single reference sensor.

respectively, extracted from each sample within the specified 0 °C to 100 °C temperature range. These reported values fall within acceptable limits for a broad range of practical IoT applications and temperature-adaptive designs [6]. Additional measurements conducted on a single reference sensor are depicted in Figure 3.8. In (a), the V_{DD} dependence of temperature inaccuracy has been extracted at 30 °C within the 300 mV 400 mV supply voltage range.

Lastly, the power consumption of each block implementing the sensor is presented in

Figure 3.8(b). It is evident that the power contribution of the TCC and the CFC is dominant, constituting approximately 85% on average of the total power consumption. Furthermore, the power consumption of the sensor is notably dependent on the actual temperature, ranging from 9.23 nW at 0 °C to 26.64 nW at 100 °C for a 350 mV supply voltage. The entire sensor consumes 7.1 nW at 25 °C when operated with a 300 mV supply voltage (23.93 nW at V_{DD} = 400 mV).

3.5 Comparison

Table 3.1: COMPARISON WITH STATE-OF-THE-ART

	JSSC'14 [21]	JSSC'16 [7]	TCASII'19 [8]	JSSC'19 [15]	JSSC'19 [14]	ISSCC'17 [16]	TCASI'21 [17]	This work
Technology	180nm	65nm	180nm	65nm	180nm	180nm	130nm	180nm
Supply Voltage [V]	1.2	1	0.9	0.5	0.8	1.2	0.95	0.35
Area [mm^2]	0.09	0.008	0.007	0.63	0.074	0.22	0.07	0.049
Measured Samples	18	7	3	12	9	16	9	9
Temperature range [°C]	0 -100	0 -100	0 -100	0 -100	-20 - 80	-20 - 80	0-80	0-100
Absolute Inaccuracy [°C]	-1.4/1.5	-0.9/0.9	-1.64/0.67	-1.53/1.61	-0.9/1.2	-0.76/0.76	-0.4/0.44	-3/3
Calibration	2-point	2-point	2-point	2 point	2-point	2-point	2-point	2-point
Resolution [°C]	0.3	0.3	0.55	0.3	0.145	90m	0.1	0.27
Conversion Time [ms]	30	0.022	300	300	839	8	59	33
Energy/Conversion [nJ]	2.2	3.4	1.2	0.23	8.9	4.56	11.56	0.46
R-FoM* [nJ·K^2]	0.19	0.3	0.36	0.02	0.19	0.037	0.116	0.034
Power [W]	71n@27°C	154µ@27°C	3.92n@27°C	763p@27°C	11n@25°C	570n	196n@30°C	14n@25°C

* R-FoM = Energy/Conversion × Resolution^2

Table 3.1 presents a comprehensive summary of the measurement outcomes for the proposed temperature sensor, compared against previous CMOS-based designs. Notably, our design distinguishes itself by operating at the lowest supply voltage. Despite prioritizing competitive resolution and power efficiency, there is, however, a trade-off with accuracy. Nonetheless, it is noteworthy that the accuracy remains within an acceptable range of ±3 °C, rendering the sensor well-suited for a variety of practical applications in the realms of Internet of Things and temperature-adaptive designs. The proposed sensor demonstrates a highly competitive Resolution Figure-of-Merit (R-FoM), calculated as $Energy/Conversion \times Resolution^2$ [18]. This is achieved while occupying a reduced silicon area, as illustrated in Figure 3.9. Specifically,

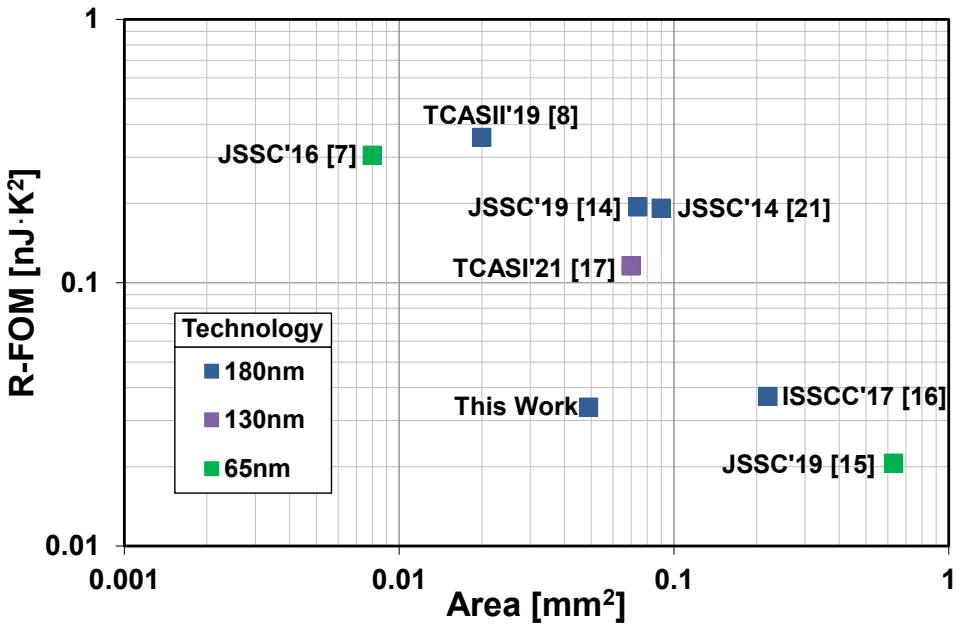

Figure 3.9: R-FOM versus area comparison.

our design emerges as the second-best in terms of silicon area occupation and the absolute best in terms of R-FoM among sensors designed in CMOS 180 nm technology. These distinctive features position the proposed sensor as an attractive candidate for integration into battery-powered, cost-effective Internet of Things devices.

3.6 Conclusion

In this chapter, an ultralow-power, fully-integrated temperature sensor designed for applications with stringent energy constraints and cost considerations was proposed. The circuit was implemented using 180 nm CMOS technology, occupying a minimal footprint of less than 0.05 mm^2. Operating at a voltage of 0.35 V, the sensor exhibits a power consumption of 14 nW at 25 °C, coupled with a competitive resolution of 0.27 °C within the temperature range of 0 °C to 100 °C, after a 2-point calibration. Remarkably, our design achieves an energy/conversion of only 0.46 nJ with a mean measured conversion time across all chips of merely 33 ms.

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IV. PROPOSED DESIGN: COMPACT TEMPERATURE SENSOR ENABLED FOR DYNAMIC THERMAL MANAGEMENT

4.1 Introduction

Temperature sensors play a critical role in facilitating dynamic thermal management (DTM) within intricate Systems on Chips (SoCs) [1–4]. Multiple sensors are strategically distributed across the die to identify potential hot or cold spots, and the collected temperature information is utilized to regulate the chip's operation within the specified thermal conditions. This ensures both optimal performance and reliability [2–4]. The maintenance of temperature safety is achieved through various adaptive strategies, including dynamic voltage and frequency scaling (DVFS), selective powering on/off of different system components, and other thermal adjustments such as fan speed regulation [1, 5, 6].

Several proposed temperature sensors [7–20] demonstrate the requisite sensing accuracy crucial for effective DTM. In the context of multi-core systems, a typical requirement includes a modest absolute inaccuracy of 8 °C and a more constrained relative inaccuracy of 3 °C [8, 21]. Furthermore, additional stipulations arise from contemporary technology trends, including aspects such as multi-processor chips, 3-D integration, and multi-supply voltage architectures [7]. Particularly:

1. Compact size is a highly desired feature to facilitate dense thermal monitoring, partic-

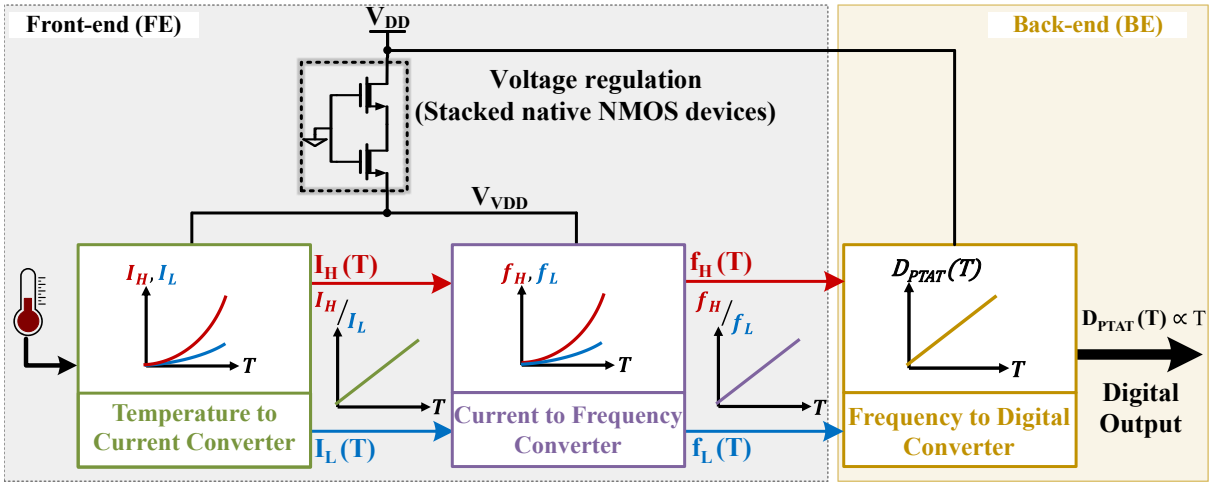

Figure 4.1: Block diagram of the temperature sensor.

ularly crucial in state-of-the-art Very Large Scale Integration (VLSI) designs. The relentless increase in the integration level of modern Systems on Chips (SoCs) has led to a rapid proliferation of potential hot and cold spots, requiring a corresponding increase in the number of temperature sensors for effective DTM. For instance, contemporary systems like POWER9 incorporate more than 60 temperature sensors [5]. Additionally, a compact footprint is essential to maintain flexibility in the design process. This is because the optimal sensor locations, often situated in close proximity to potential hot or cold spots, are typically identified in the later stages of the design phase and are commonly within densely populated areas of the chip [8].

2. Robustness is paramount in the context of temperature sensors. It is expected for a temperature sensor to preserve its sensing accuracy despite variations in voltage and manufacturing processes. Overestimating the temperature may result in unnecessary performance throttling, while underestimating can lead to reliability issues. Therefore, ensuring resilience to these variations is critical for the effective and reliable operation of temperature sensors.

3. Another critical requirement is broad supply voltage scalability [7]. In contemporary SoCs, Dynamic Voltage and Frequency Scaling (DVFS) techniques are frequently employed to fine-tune performance while managing power consumption, particularly for the digital components of the system. The supply voltage can be dynamically adjusted, sometimes down to near-threshold levels, to save energy when reduced performance is acceptable. Therefore, it is highly desirable for temperature sensors to support supply voltage scalability, allowing them to share the same power grids with digital circuits. Unfortunately, some previously proposed temperature sensors have proven to be insufficiently voltage scalable [9, 11, 14–16, 19], and/or do not support sub-1 V operation [8, 15–17, 19, 22].

This chapter introduces a small-area fully-integrated CMOS temperature sensor designed for precise placement in close proximity to target hot or cold spots within Systems on Chips. The sensing circuit, characterized by low complexity and PMOS-based architecture, converts the local temperature into two sub-threshold biasing currents. These currents are utilized to establish two oscillation frequencies, whose linearly increasing ratio serves as an indicator of temperature. The frequency ratio is subsequently translated into a digital output code through a digital backend employing binary counters. The proposed design features a simple embedded line regulation mechanism, enabling operation across a wide power supply range. This versatility makes it particularly appealing for systems supporting multi-supply voltages and/or Dynamic Voltage and Frequency Scaling (DVFS). Fabricated in $180\,\mathrm{nm}$ CMOS technology for the targeted temperature range of $0\,^{\circ}\mathrm{C}$ to $100\,^{\circ}\mathrm{C}$, the design exhibits a compact footprint of approximately $0.02\,\mathrm{mm}^2$ and operates within a supply voltage range of 0.6V to 1.8V. Moreover, it consumes less than $1.6\,\mu\mathrm{W}$ (V_{DD}=0.6V and $Temp$=$25\,^{\circ}\mathrm{C}$), with an energy per conversion

of 1.05 nJ. The achieved results demonstrate an inaccuracy constrained within $\pm 1.4\,^{\circ}\mathrm{C}$ and a resolution of $0.24\,^{\circ}\mathrm{C}$.

4.2 Temperature sensor architecture

Derived from the temperature-to-digital conversion methodology employed in [13, 14], the sensor relies on three primary processing blocks, as illustrated in Figure 4.1: 1) Temperature-to-Current Converter (TCC) This component serves as the sensing element in the proposed circuit. It generates two sub-threshold currents, I_H and I_L (where $I_H > I_L$), and their ratio I_H/I_L exhibits a linear increase with temperature. 2) Current-to-Frequency Converter (CFC): Comprising two independent ring oscillators controlled by mirrored I_H and I_L currents, the CFC ensures that the ratio of the two oscillation frequencies (f_H/f_L) maintains a linear relationship with temperature. 3) Frequency-to-Digital Converter (FDC): This block is responsible for generating the digital temperature code based on the f_H/f_L ratio.

The voltage scalability of the sensor is facilitated by two stacked native (i.e., zero threshold voltage transistors) NMOS devices [12]. These transistors provide line regulation for the supply-sensitive TCC and CFC blocks. These blocks operate in the sub-threshold regime, powered by an almost stable virtual V_{DD} (V_{VDD}), regardless of the actual V_{DD} and temperature. In our 180 nm implementation, the V_{VDD} remains approximately 440 mV across a wide range of temperatures ($0\,^{\circ}\mathrm{C}$ to $100\,^{\circ}\mathrm{C}$) and power supply variations (0.6V to 1.8V). In contrast, the FDC circuit, being based on non-critical digital circuitry (inherently more robust to temperature and voltage variations), is powered directly by V_{DD}.

4.2.1 Temperature-to-Current Converter

The Proportional-to-Absolute-Temperature (PTAT) behavior of the current ratio I_H/I_L is achieved through the low-complexity circuit depicted in the inset of Figure 4.2. This circuit consists of two branches, each incorporating only five diode-connected PMOS devices. The selection of PMOS only transistors for this design was to improve robustness against process variation, by being of the same device type all transistors will experience the same variation. The left branch is implemented with three identically sized transistors, while the right branch employs two transistors. This configuration ensures that the virtual supply voltage (V_{VDD}) is equally partitioned between the transistors, resulting in $V_{SG} = V_{VDD}/3$ for the left branch and $V_{SG} = V_{VDD}/2$ for the right branch.

Since all the devices in the TCC operate in the sub-threshold region, with a source-to-drain voltage (V_{SD}) larger than four thermal voltages (V_T = k_BT/q where k_B is the Boltzmann constant, T is the absolute temperature, and q is the electron charge), their source current I_S can be expressed as [23]:

$$I_S = \frac{W}{L} I_0 \, exp\left(\frac{q(|V_{GS}| - |V_{th}|}{nk_BT}\right), \tag{31}$$

where W/L is the aspect ratio of the device, I_0 is the technology dependent subthreshold current which can be obtained by extrapolating the current for $V_{GS} = V_{th}$, V_{th} is the threshold voltage and n is the subthreshold factor.

Thus, the current ratio I_H/I_L can be written as:

$$\frac{I_H}{I_L} = \frac{\left[\frac{W}{L}\right]_1}{\left[\frac{W}{L}\right]_2} \, exp\left(-\frac{qV_{VDD}}{6nk_B} \cdot \frac{1}{T}\right), \tag{32}$$

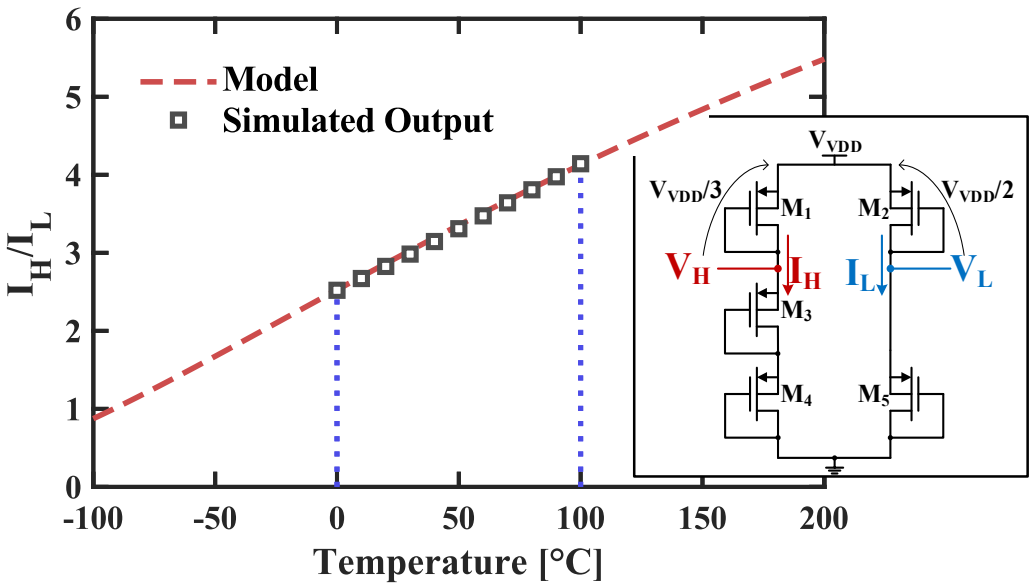

Figure 4.2: Simulated I_H/I_L current ratio as a function of the temperature. In the inset: the temperature-to-current converter (TCC) circuit.

In the equation above, we have assumed that I_0 and V_{th} for transistors M1 and M2 are identical.

Given the value assumed by the term $-qV_{VDD}/6nk_B$, the exponential term can be effectively approximated by a linear relation within a limited temperature range (e.g., 0 °C to 100 °C), as follows:

$$\frac{I_H}{I_L} \approx m \times Temp + p, \tag{33}$$

with m = 0.0158 $1/\,^{\circ}\mathrm{C}$, p = 2.55 for our design, and $Temp$ expressed in °C. The model equation (32) has been plotted in Figure 4.2, demonstrating the good agreement with simulation results.

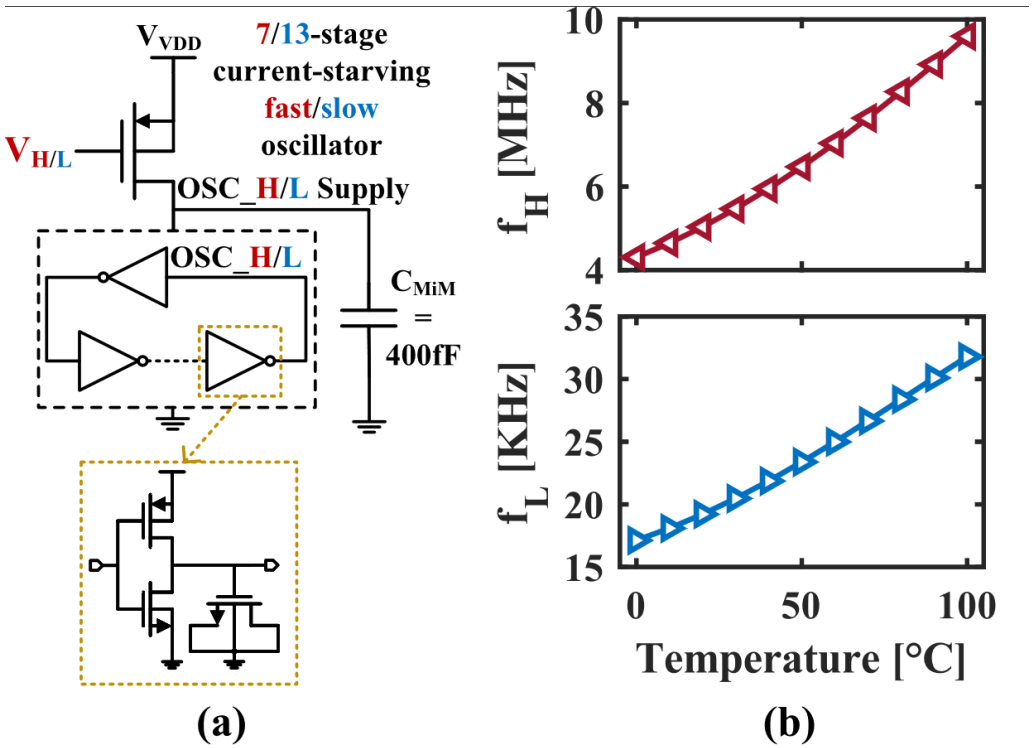

Figure 4.3: (a) Current-to-frequency converter (CFC), (b) simulated f_H and f_L vs temperature.

4.2.2 Current-to-Frequency Converter

As illustrated in Figure 4.3(a), the CFC utilizes two current-starved ring oscillators to transform the mirrored version of the I_H and I_L currents into two digital pulse signals. The frequency ratio f_H/f_L of these signals exhibits a linear Proportional-to-Absolute-Temperature (PTAT) trend.

In general, the oscillation period T_{osc} of a current-biased ring oscillator can be expressed as [13]:

$$T_{osc} = N\left(\frac{C_L \Delta V}{I_{bias}} + t_{fall} + t_{rise}\right) \tag{34}$$

where N is the number of stages in the ring oscillator, C_L is the load capacitance of a single delay cell, ΔV is the output voltage amplitude, I_{bias} is the biasing current, while t_{fall} and t_{rise}

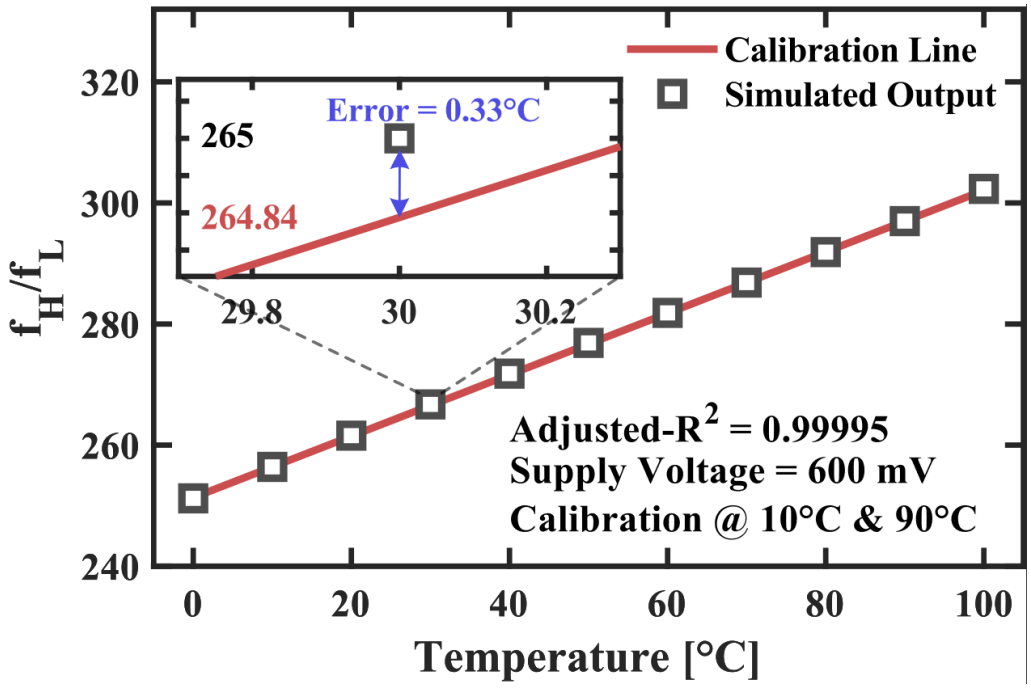

Figure 4.4: Simulated f_H/f_L frequency ratio as a function of temperature in the 0 °C–100 °C range, V_{DD} = 600 mV.

are the falling and the rising times of a single stage. For an accurate approximation of the oscillation frequency, both t_{fall} and t_{rise} must be significantly smaller than $(C_L \Delta V)/I_{bias}$. In this specific case, the ratio f_H/f_L $(= T_{osc,L}/T_{osc,H})$ demonstrates a comparable PTAT characteristic as I_H/I_L.

In the proposed architecture, both ring oscillators employ an identical delay cell topology, as depicted in Figure 4.3(a). This configuration relies on a standard CMOS inverter loaded by a NMOS capacitor. This capacitor serves the dual purpose of constraining the oscillation frequency and preventing an unwarranted escalation in the number of delay cells. Moreover, the augmented capacitance at the output node of each inverter contributes to enhancing the linearity of the oscillation frequency concerning the biasing current, as articulated in equation (4).

To achieve a balance between accuracy and efficiency, the two ring oscillators have been

optimized with an adequate number of stages (13 and 7 for the slow and fast oscillators, respectively) and accordingly chosen delay stage sizes. As illustrated in Figure 4.3(a), decoupling MIM capacitors (400 fF) have been incorporated at the supply voltage nodes of the two oscillators. This addition aims to mitigate the impact of switching noise on the oscillation frequency, hence, enhancing the overall robustness and performance of the sensor.

Simulations of the FDC circuit driven by the TCC are depicted in Figure 4.3(b) and Figure 4.4. In Figure 4.3(b), the variation in temperature from 0 °C to 100 °C corresponds to a frequency range of f_L (f_H) spanning from 17 kHz (4.3 MHz) to 31.8 kHz (9.6 MHz). As illustrated in Figure 4.4, the high adjusted-R^2 value of 0.99995, evaluated on the f_H/f_L ratio, substantiates the acceptability of the error post a two-point calibration, with temperature references set at 10 °C and 90 °C.

4.2.3 Voltage Regulation

A simplified voltage regulation mechanism has been incorporated to enhance the line and temperature sensitivities of the TCC and CFC blocks. This enhancement involves the insertion of two series-connected native NMOS devices between V_{DD} and the TCC+CFC circuits, as illustrated in Figure 4.1. Consequently, the source of the lower native transistor corresponds to the virtual supply voltage V_{VDD} perceived by the TCC and CFC blocks. Notably, the stack of two native transistors consistently operates in the sub-threshold region, given that both have $V_G = V_{th} = 0V$ and $V_S > 0V$. Employing two long-channel transistors in series for the voltage regulator block renders its $I(V,T)$ characteristic largely immune to variations in external V_{DD}. Furthermore, this approach results in an almost constant V_{VDD} despite temperature fluctuations. To explain this, refer to the diagram in Figure 4.5, where the regulator (REG) and the TCC and CFC circuits (LOAD) are modeled independently. For the regulator, an $I(V,T)$ characteristic

is assumed in the following form:

$$I_R = \alpha_R(T)\, exp\left(\frac{-q\, V_{VDD}}{\beta_R(T)\, k_B T}\right), \tag{35}$$

in which the DIBL effect is neglected (i.e., the V_{DS} impact on I_D).

This type of regulator is capable of providing an almost constant V_{VDD} to load a circuit whose $I(V,T)$ relation can be expressed as follows:

$$I_L = \alpha_L(T)\, exp\left(\frac{q\, V_{VDD}}{\beta_L(T)\, k_B T}\right), \tag{36}$$

which is appropriate for CMOS circuits operating in the sub-threshold regime, as is the case for the TCC and CFC blocks in our design.

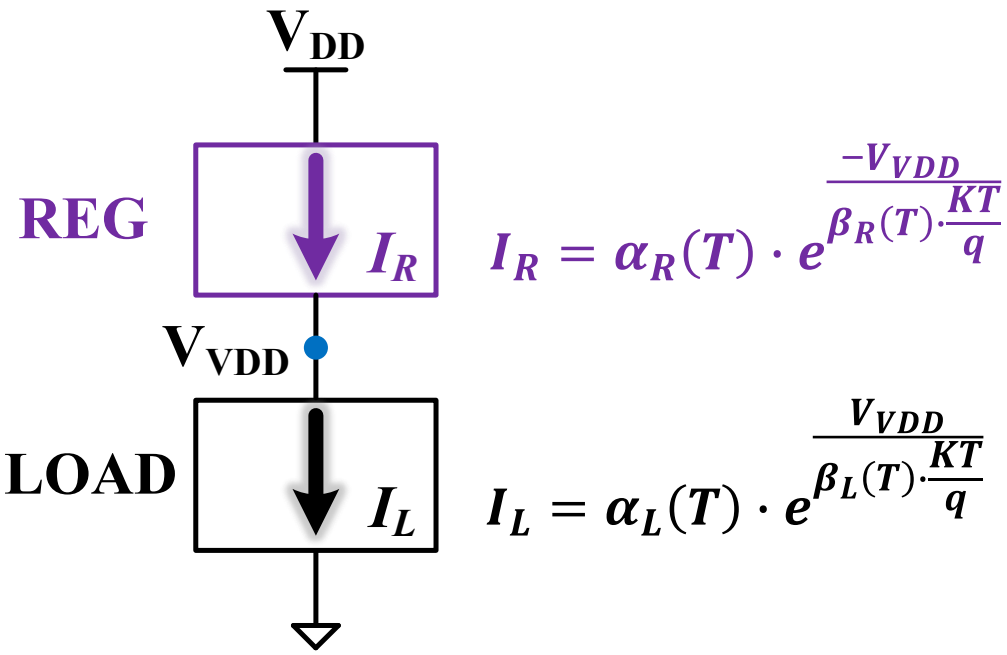

Figure 4.5: Regulator and loading circuits model equations for the temperature sensitivity characterization of the V_{VDD}.

Figure 4.6 illustrates the DC V-I curves for both the regulator and the load, simulated at

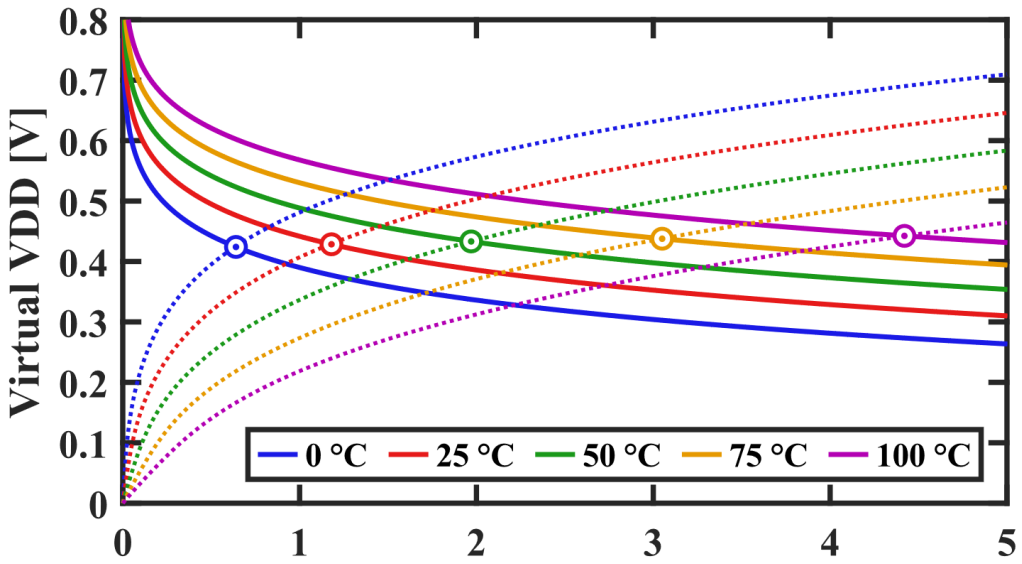

Figure 4.6: Load curves of regulator and loading circuits at different temperatures.

various temperatures. Analytical expressions of these curves can be derived by converting (35) and (36) into their logarithmic forms. The intersection points between the two families of curves denote the load conditions for different temperatures. This plot provides a clear visual representation of how V_{VDD} remains essentially stable with temperature variations, even as the supply current exhibits exponential growth with temperature.

Analytically, by manipulating (35) and (36), V_{VDD} can be expressed as follows:

$$V_{VDD} = \beta_{eq}(T)\,\frac{k_B T}{q}\,log\left(\frac{\alpha_R(T)}{\alpha_L(T)}\right) \tag{37}$$

$$\text{with } \beta_{eq} = \frac{\beta_L\,\beta_R}{\beta_L + \beta_R}\,, \tag{38}$$

In this expression, each term, including β_{eq}, $\frac{k_B T}{q}$, α_R, and α_L, are a function of temperature. Notably, we observed that the ratio $\frac{\alpha_R}{\alpha_L}$ remains approximately constant, and the β_{eq} term exhibits an almost 1/T dependence, effectively compensating for the linear term in $\frac{k_B T}{q}$. The

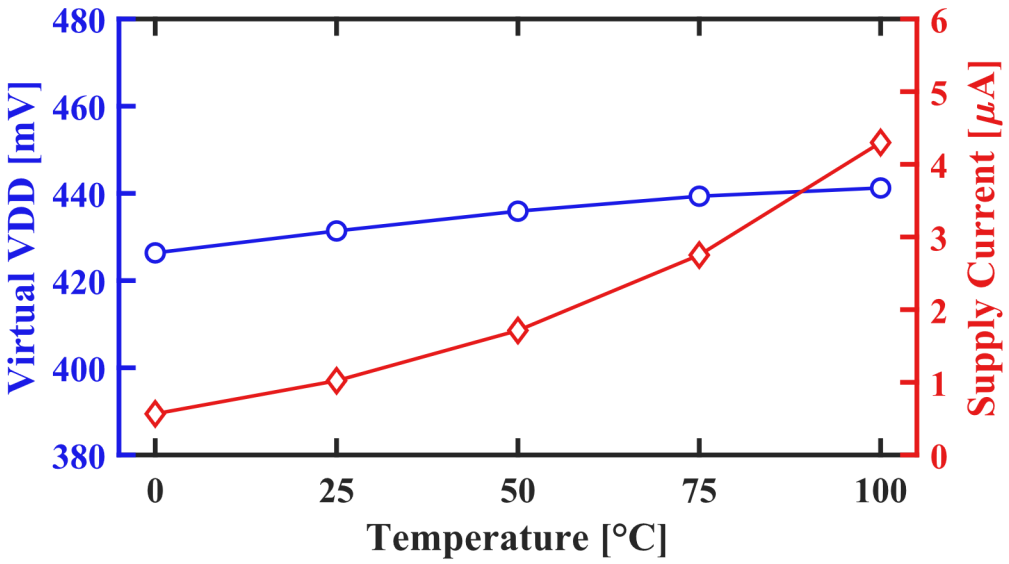

Figure 4.7: Model equations of the V_{VDD} and supply current drawn by the TCC and CFC blocks as a function of the temperature.

fitting parameters for both the regulator and load circuits were extracted at various temperatures. The analytical expressions for V_{VDD} and the supply current are presented in Figure 4.7. Notably, as the temperature increases from 0 °C to 100 °C, despite observing approximately a 7x increase in current, the corresponding voltage change is only about 3%. The extracted model equations align with the simulations of the sensor front-end, as illustrated in Figure 4.8. This figure depicts the behavior of the V_{VDD} voltage node and the current drawn by the front-end sensor circuitry, which comprises stacked native NMOS devices biasing TCC and CFC blocks, as functions of temperature for V_{DD} ranging from 0.6 V to 1.8 V in 100 mV increments. Notably, the average current increases from about 0.6 μA at $T = 0\,°\mathrm{C}$ to 4.1 μA at $T = 100\,°\mathrm{C}$, corresponding to a more than 6.9x increase in drawn current as the temperature rises from 0 °C to 100 °C. Despite this significant current variation, V_{VDD} increases by less than 5% over the same temperature range. Furthermore, V_{VDD} remains relatively constant for V_{DD} values ranging from 0.6 V to 1.8 V. These results highlight the advantages of the adopted low-complexity

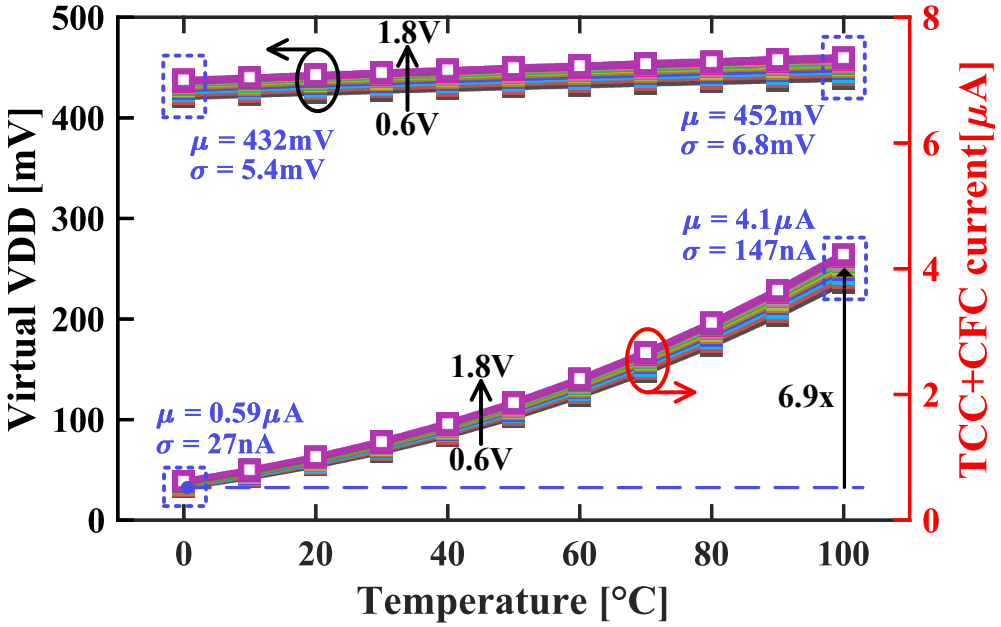

Figure 4.8: Simulated Virtual V_{DD} and temperature-to-current converter + current-to-frequency converter drawn current for supply voltage ranging from 0.6 V to 1.8 V.

voltage regulation in improving both line and temperature sensitivities.

In deeply scaled process nodes, typically below 40-nm, native MOSFETs may not be readily available. In such instances, the outlined voltage regulation can be implemented using nMOS devices with regular threshold voltage (RVT), provided they are appropriately sized and biased with a stable gate voltage near the threshold, ensuring that $V_S > 0$, and thereby enabling them to operate in the sub-threshold regime.

4.2.4 Frequency-to-Digital Converter

The schematic representation of the digital back-end, responsible for generating the digital PTAT code, is illustrated in Figure 4.9. Given that the amplitudes of the signals produced by the two ring oscillators in the CFC are confined by the V_{VDD} voltage level, both $OSC_{H,L}$ signals experience an up-conversion to the V_{DD} voltage domain. This conversion is facilitated

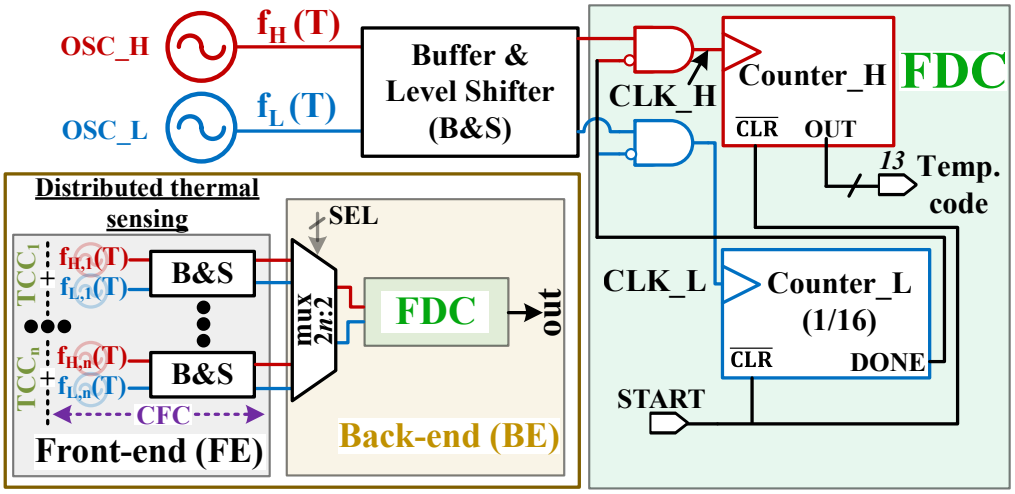

Figure 4.9: Frequency-to-digital converter architecture. The inset shows the principle scheme for distributed thermal sensing.

by the compact and energy-efficient level shifter (LS) proposed in [24]. The circuit demonstrates a substantial voltage conversion range and adapts effectively to variations in the V_{DD} voltage level [24], ensuring full compatibility with DVFS systems. The subsequent step involves frequency-to-digital conversion through two asynchronous counters. The $Counter\_L$ serves as the reference counter to establish the time window for sampling temperature measurements. This 5-bit counter define a sampling time window of $16/F_L$ seconds, utilizing only 4 bits for counting while the MSB is employed for triggering purposes. Conversely, the resolution of the temperature sensor is contingent on $Counter\_H$, which has been configured as a 13-bit counter to prevent counting overflow across the temperature detection range from 0 °C to 100 °C, accounting for potential offsets due to process and mismatch variations.

The timing diagram of the FDC block is depicted in Figure 4.10. Upon triggering the START signal (it is worth mentioning that the START and OSC_L signals are synchronized), both counters commence counting upwards until the DONE signal transitions to '1' (signifying the MSB of the reference counter). This occurs after sixteen cycles of the slower oscillator.

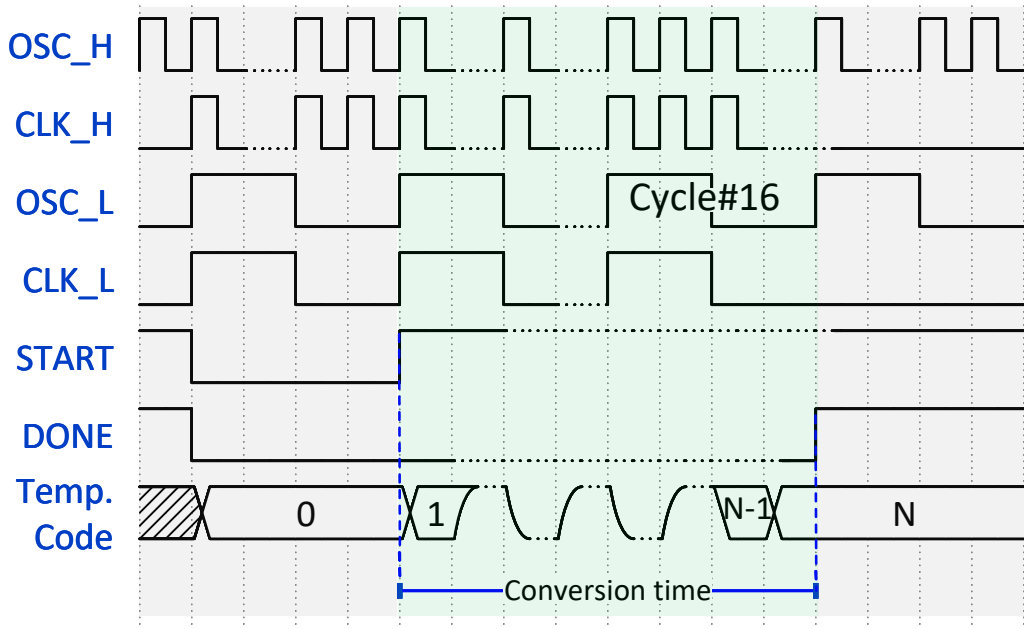

Figure 4.10: Timing diagram of the FDC block.

Subsequently, a temperature code becomes available at the output of $Counter\_H$. The counters are reset by the START signal when a new temperature measurement is necessitated.

In a typical system configuration, the FDC circuit can be shared among multiple sensor front-ends, as illustrated in the schematic in Figure 4.9. In such a setup, the back-end incorporates two n-to-1 multiplexers responsible for selecting n output pairs from various sensor front-ends. Each pair consists of the two signals corresponding to f_H and f_L frequencies. The selected pair is then routed to the shared FDC. This design enables the conservation of valuable silicon area when multiple thermal information outputs are needed for an efficient Dynamic Thermal Management strategy.

The simulated inaccuracy of the output temperature code within the specified temperature detection range is illustrated in Figure 4.11. Different process corners are considered, and a two-point calibration is applied using temperature references of 10 °C and 90 °C. At 50 °C, an absolute inaccuracy ranging from -1.14 °C to 1.16 °C is observed for the FS/SF corners. This

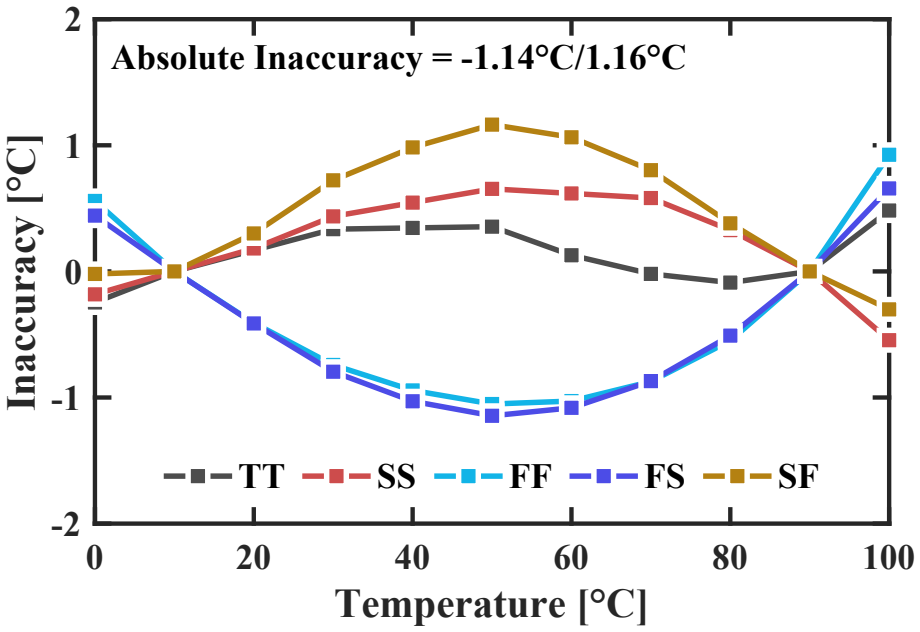

Figure 4.11: Simulated inaccuracy as a function of temperature for different process corners. Temperature calibration points: 10 °C and 90 °C.

outcome indicates a low sensitivity of the proposed design to process variability.

4.3 Experimental Results

The fully-integrated temperature sensor was implemented in a 180 nm CMOS technology node, featuring a remarkably compact silicon footprint of less than 0.021 mm^2. The physical design details are depicted in Figure 4.12(a), and a micrograph of the test chip is presented in Figure 4.12(b). The voltage-regulated sensor front-end occupies a silicon area of 14650 $\mu\mathrm{m}^2$, while the FDC circuit has a footprint of approximately 6300 $\mu\mathrm{m}^2$.

Twenty test chips were measured within the designated temperature range, employing a two-point calibration strategy with temperature references set at 10 °C and 90 °C. The results are presented in the following. Figure 4.13 illustrates the temperature code of the measured chips calibrated for V_{DD}=600 mV. Good linearity was observed across all samples, evidenced

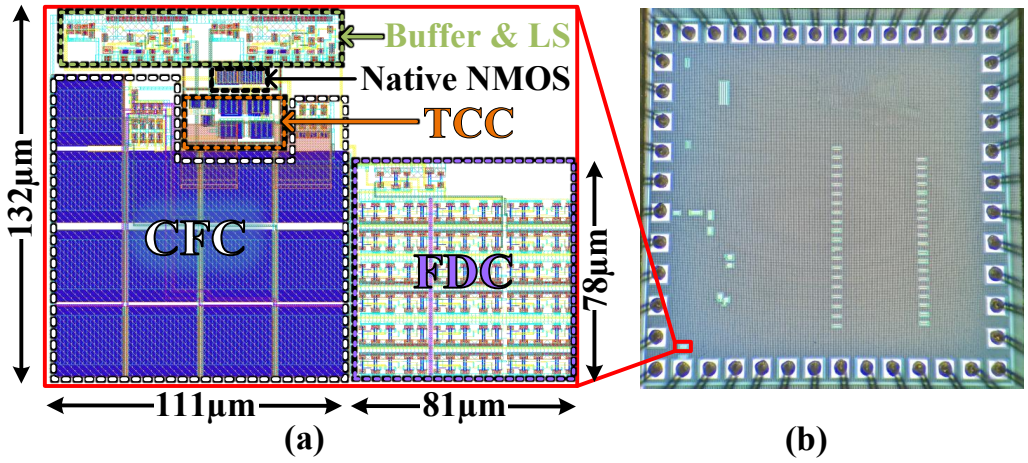

Figure 4.12: (a) Layout of the designed temperature sensor and (b) micrograph of the test chip.

by an average adjusted-R^2 of 0.9997. This performance, while slightly diminished compared to simulation results depicted in Figure 4.4 is still competitive. A discernible difference in the slope coefficient among individual samples is evident from Figure 4.13 showing a standard deviation $\sigma = 4.17/\,^{\circ}\mathrm{C}$ among the measured slopes for all chips. This disparity prevents the application of a one-point calibration method, particularly when a significantly high level of measurement accuracy is imperative. The temperature-dependent inaccuracy of the measurements is depicted in Figure 4.14. Across all measured samples, the inaccuracy consistently falls within the range of –1.4 °C to 1.4 °C. Even when considering the pessimistic 3σ (approximately $\pm$ 2.5 °C) data calculated from the inaccuracy across the 20 samples. The obtained measurement results align comfortably within the acceptable accuracy specifications for an effective DTM in state-of-the-art System-on-Chip (SoC) designs [8, 21]. Further tests were conducted on a single sensor, and the outcomes are presented in Figure 4.15 and Figure 4.16. This involved evaluating the impact of voltage scaling through a systematic sweep the supply voltage, ranging from 0.6V to 1.8V in 100 mV increments. It is important to note that, for each supply voltage, an independent two-point calibration was applied. As depicted in Figure 4.15,

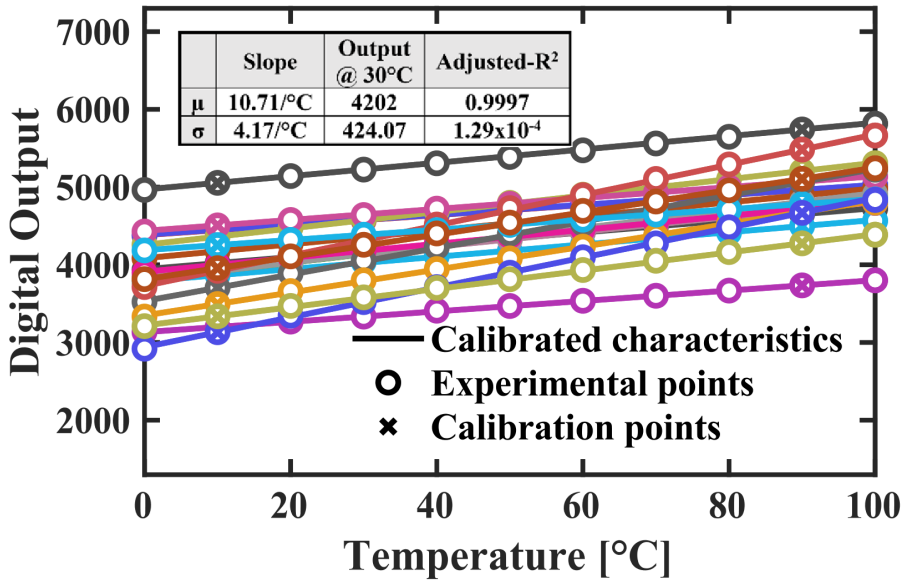

Figure 4.13: Measured digital output as a function of the temperature for V_{DD} = 0.6 V in 20 test chips.

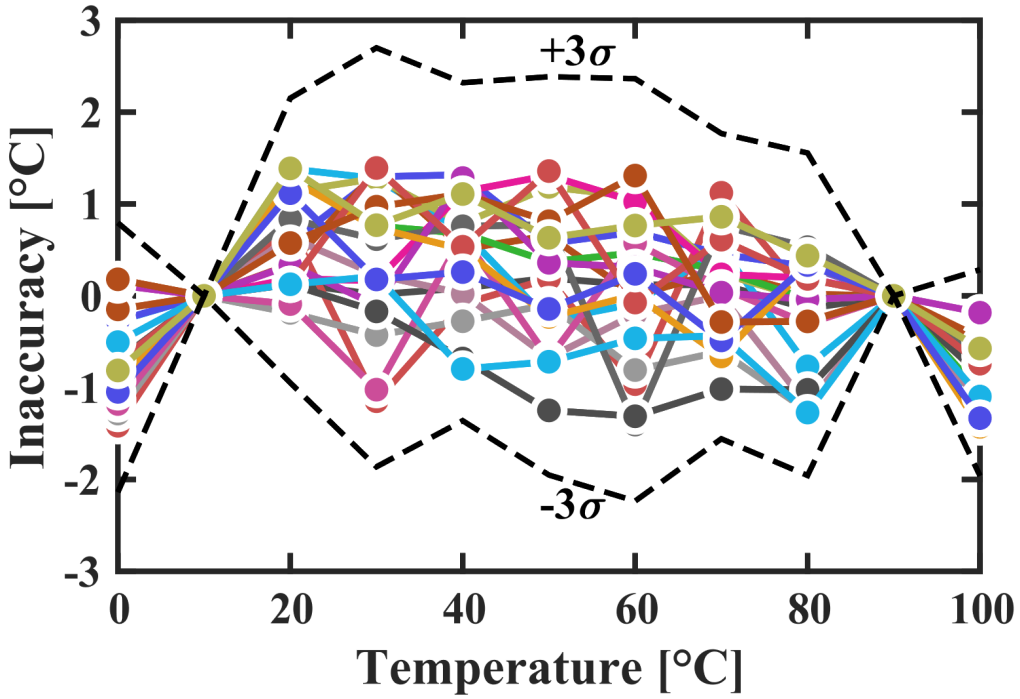

Figure 4.14: Measured digital output inaccuracy as a function of the temperature for V_{DD} = 0.6 V in 20 test chips.

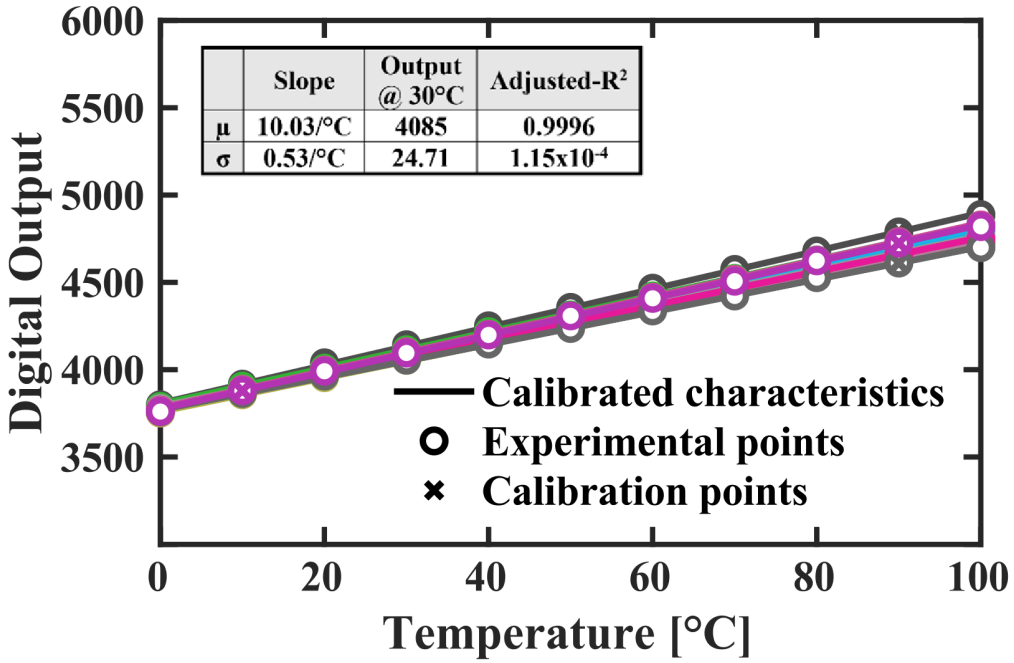

Figure 4.15: Measured digital output for a typical sample as a function of the temperature over the 0.6 V– 1.8 V supply voltage range.

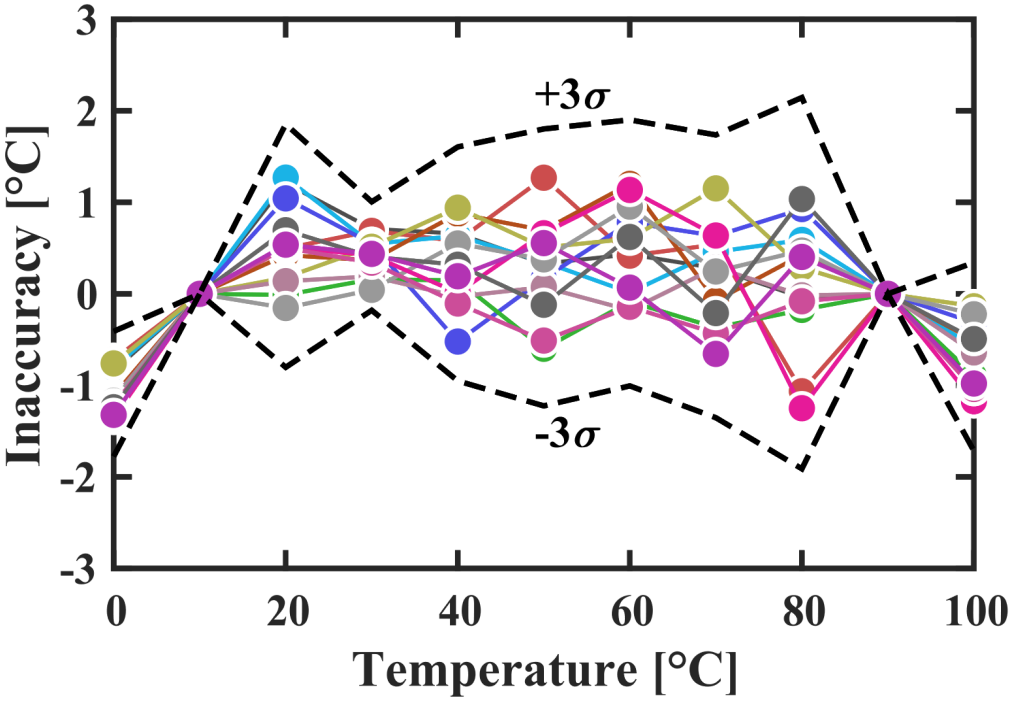

Figure 4.16: Measured digital output inaccuracy for a typical sample as a function of the temperature over the 0.6 V– 1.8 V supply voltage range.

variations in the digital temperature code are particularly noticeable only at elevated temperatures, while for the lower temperatures the sensor output is closer despite the supply voltage change, as confirmed by the low value of σ=0.53/ $^{\circ}$C. Concurrently, Figure 4.16 showcases the inaccuracy, ranging from –1.35 $^{\circ}$C at V_{DD} = 1.5V to 1.27 $^{\circ}$C at V_{DD} = 0.8V. The 3σ inaccuracy remains within the $\pm$2 $^{\circ}$C range, affirming the robustness of the measurements across varying supply voltages.

The die-to-die variability within the designated temperature detection range is shown in Figure 4.17(a-c), encompassing all test samples and four distinct supply voltage values, namely V_{DD}=0.6 V, 1 V, 1.4 V, and 1.8 V. In Figure 4.17(a), the peak inaccuracy is confined within a range of 1.1 $^{\circ}$C to 1.45 $^{\circ}$C, with a median value approaching 1.3 $^{\circ}$C. Correspondingly, the Root Mean Square (RMS) inaccuracy ranges from 0.42 $^{\circ}$C to 0.89 $^{\circ}$C, as delineated in Figure 4.17(b). Notably, the achieved resolution, defined as the inverse slope of the sensor output characteristics, demonstrates highly competitive values, with a worst-case scenario of 0.22 $^{\circ}$C observed for V_{DD} = 1.8 V, as illustrated in Figure 4.17(c). The average resolution across measurements stands at 0.132 $^{\circ}$C, 0.131 $^{\circ}$C, 0.138 $^{\circ}$C, and 0.139 $^{\circ}$C for V_{DD} values of 0.6 V, 1 V, 1.4 V, and 1.8 V, respectively.

The potential impact of thermal noise on the sensor's resolution is further tested through an experiment where the temperature code is measured 200 times at a fixed temperature of 25 $^{\circ}$C for a typical sample, as depicted in Figure 4.18. The standard deviation (σ) of the samples is found to be 0.24 $^{\circ}$C, indicative of the noise-limited resolution. This corresponds to 1.84 Least Significant Bit (LSB), providing insights of the achievable precision in the presence of thermal noise.

The sensitivity to unwanted voltage variations for the typical sample is meticulously char-

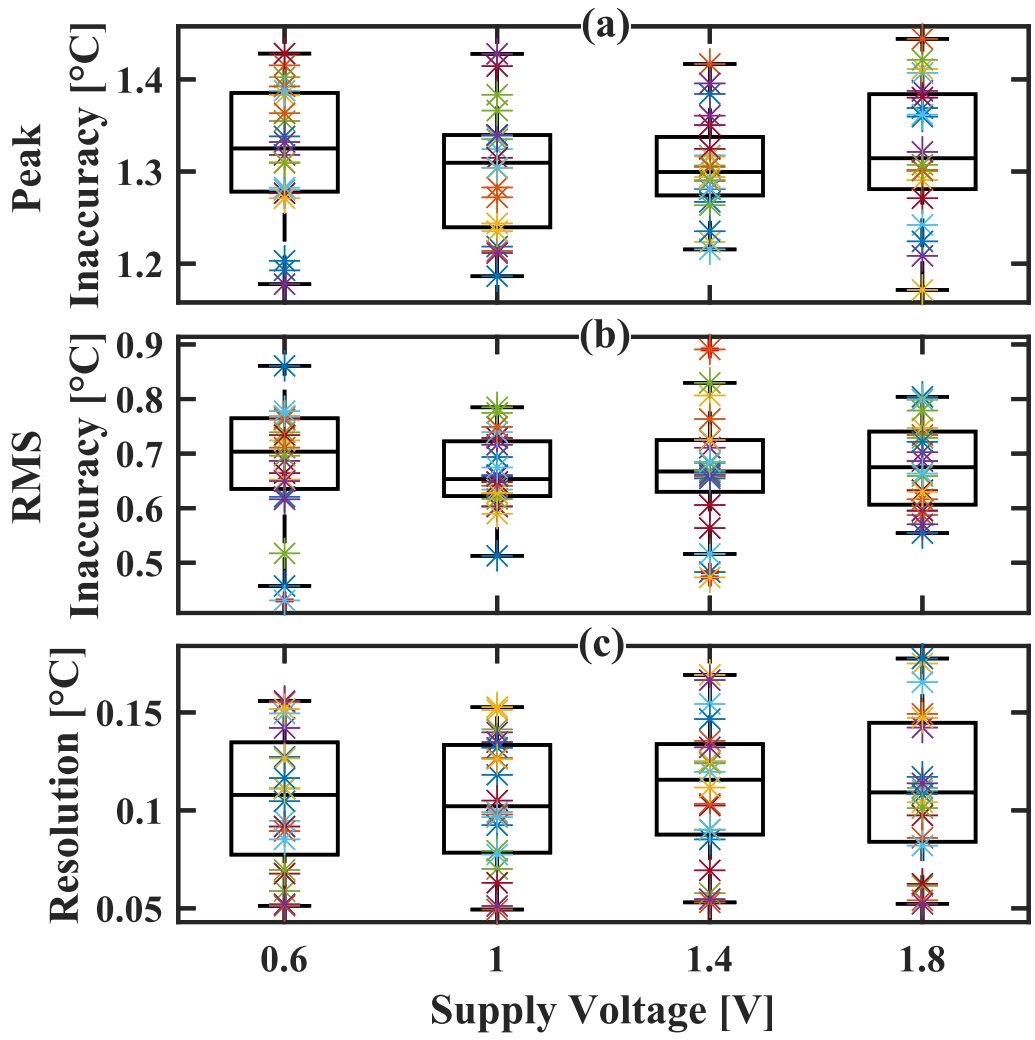

Figure 4.17: Measured peak inaccuracy (a), RMS inaccuracy (b) and resolution (C) for different supply voltages and 20 test chips.

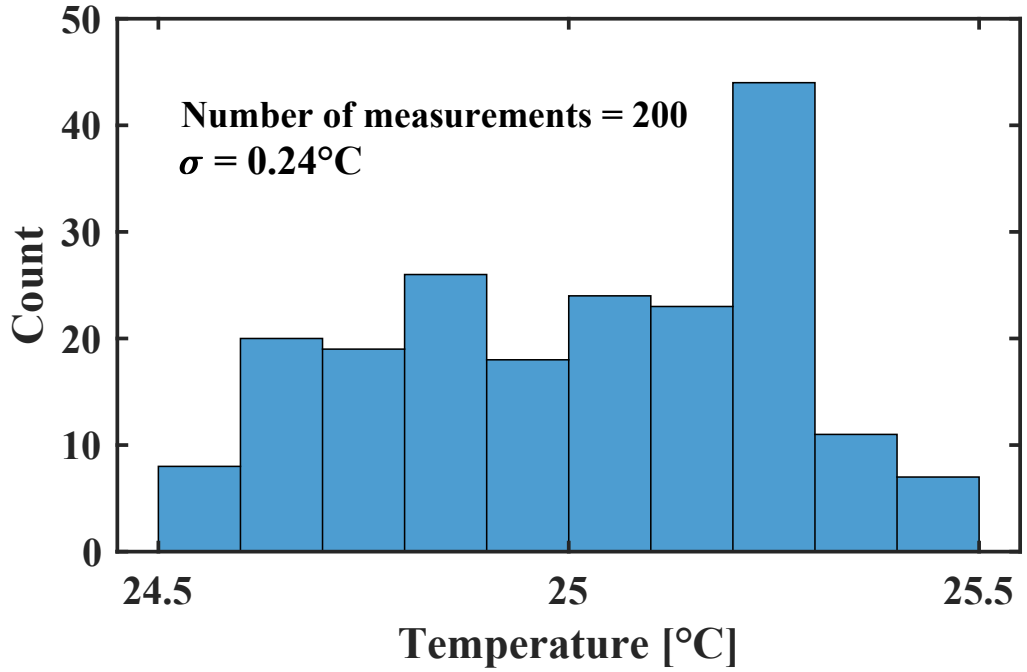

Figure 4.18: Measured histogram of 200 different temperature readings at temperature T =25 °C.

acterized in Figure 4.19, presenting the inaccuracy as a function of supply voltage. A line sensitivity of 8.21 °C/V at a temperature of 30 °C is determined by calibrating the sensor at 0.9 V and subsequently extracting the inaccuracy when the supply voltage undergoes changes in the ±200 mV range (equivalent to ±22%). However, in scenarios where the supply voltage of the sensor is altered due to Dynamic Voltage and Frequency Scaling (DVFS) adjustments, the line sensitivity can be further reduced to 0.56 °C/V at 30 °C. In this context, two temperature calibration points for each potential V_{DD} (within the chip's operational V_{DD} range) can be conveniently pre-stored to establish the actual calibrated characteristic, as illustrated in Figure 4.16. This approach enables the sensor to effectively mitigate the impact of DVFS-induced supply voltage variations, enhancing its robustness and maintaining a more consistent level of accuracy under varying operating conditions.

Lastly, Figure 4.20 presents the power consumption profile of the proposed sensor as a func-

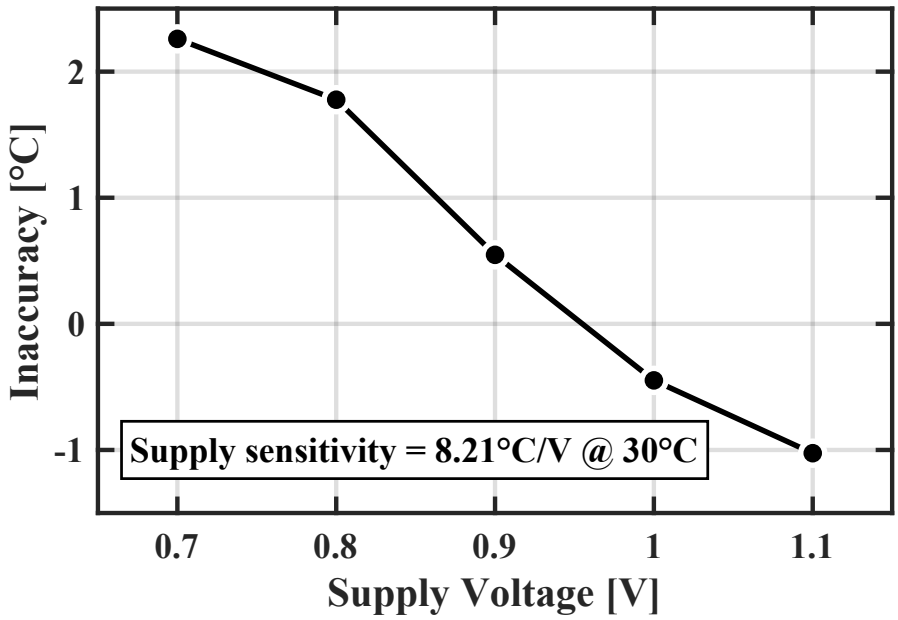

Figure 4.19: Measured inaccuracy vs supply voltage at temperature $T = 30\,^{\circ}\mathrm{C}$. For this measurement the sensor was calibrated only at $0.9\,\mathrm{V}$.

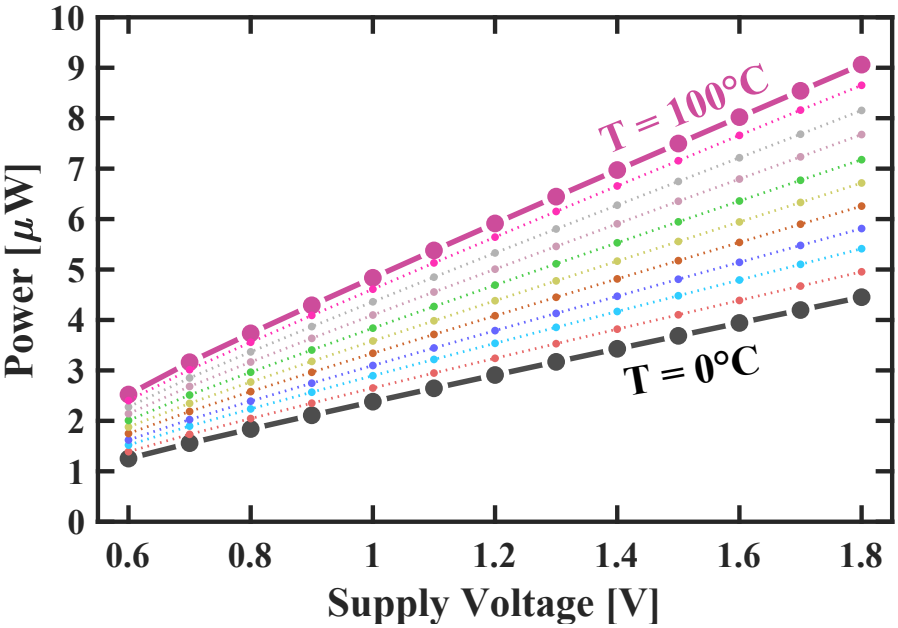

Figure 4.20: Measured power as a function of supply voltage for temperature spreading from $0\,^{\circ}\mathrm{C}$ to $100\,^{\circ}\mathrm{C}$.

tion of V_{DD} across a temperature range from 0 °C to 100 °C. The power consumption exhibits nearly linear growth with V_{DD}, ranging from 1.57 μW (V_{DD} = 0.6V) to 5.61 μW (V_{DD} = 1.8V) at 25 °C. Conversely, power consumption also shows an increase with temperature, peaking at approximately 9 μW (V_{DD}= 1.8V and $Temp$= 100 °C). This characterization provides valuable insights into the power performance of the sensor, crucial for optimizing energy efficiency in various applications across a broad temperature range.

4.4 Comparison

Table 4.1 provides a summary of the measurement results for the temperature sensor, comparing it to alternative CMOS designs sourced from various references [8–11, 13–16, 19, 25, 26]. The experimental data for our design is derived from measurements on 20 test chips, offering a robust statistical foundation, whereas most competitor designs are based on a smaller number of samples (except for [8] and [26]).

Circuits reported in [8, 15, 16, 19] lack support for operation with sub-1 V voltages, and sensors discussed in [9, 14–16] exhibit poor voltage scalability. In contrast, our sensor demonstrates versatility by supporting a larger supply voltage operating range, spanning from 0.6 V to 1.8 V, and showcases a supply sensitivity of approximately 8 °C/ V. Notably, our design does not need any external reference signal, a feature present in circuits reported in [25] and [26], as well as the absence of a reference voltage as required in [25], respectively.

Furthermore, the proposed design exhibits a relatively compact footprint of just 0.021 mm^2, positioning it as the least area-intensive design in the 180 nm technology node and the third smallest in absolute terms. This compact form factor enhances the practicality and integration potential of the proposed temperature sensor in various applications.

Table 4.1: COMPARISON WITH THE STATE-OF-THE-ART

	SENSORS'14 [16]	JSSC'16 [9]	SENSORS'17 [15]	SENSORS'18 [19]	JSSC'19 [10]	JSSC'19 [13]	TCASI'21 [27]	ACCESS20 [8]	JSSC'20* [26]	SSC-L'20* [25]	TCAS-II'21 [14]	This work
Technology [nm]	130	65	180	130	65	180	130	65	55	65	180	180
Measured Samples	7	7	8	10	12	9	9	35	64	9	9	20
Voltage Scalability (Voltage Operating Range [V])	No	Yes (0.85 – 1.05)	No	Yes (1.05 – 1.4)	Yes (0.5 – 1)	Yes	No	Yes (1 – 1.5)	Yes (0.8 – 1.3)	Yes (0.7 – 1.05)	No	Yes (0.6 – 1.8)
Reference Supply Voltage [V]	1.2	1	1.8	1.2	0.5	0.8	0.95	1.2	0.9	0.8	0.35	0.6
Area [mm^2]	0.031	0.0082 (0.004 + 0.0042$^{(a)}$)	0.118	0.06	0.63	0.074	0.07	0.0019	0.0388 (0.0018 + 0.037$^{(a)}$)	0.32	0.049	0.021 (FE: 0.0147 BE:0.0063)
Temperature range [°C]	20 – 120	0 – 100	-20 – 120	-20 – 100	0 – 100	-20 – 80	0 – 80	-10 – 100	-40 – 125	-30 – 70	0 – 100	0 – 100
Off-Chip non-linearity correction	Yes	Yes	No	No (Yes)	No	No	Yes	Yes	Yes	No	No	No
Calibration	1-point	2-point	2-point	1-point	2-point	2-point	2-point	2-point	2-point	2-point	2-point	2-point
Min/Max Inaccuracy [°C]	-0.63/1.04	-0.9/0.9	-1.5/1.71	-2.88/2.71 (-1.7/1.26)	-1.53/1.61	-0.9/1.2	-0.4/0.44	-1.62/2.04	-0.37/0.72	-1/0.7	-3/3	-1.45/1.4
Relative Inaccuracy[(b)] [%]	1.67	1.8	2.86	4.66 (2.55)	3.14	2.1	1.05	4.54	0.66	1.7	6	2.85
Resolution [°C]	0.595$^{(e)}$	0.3$^{(f)}$	0.048$^{(f)}$	0.34$^{(e)}$	0.3$^{(e)}$	0.145$^{(f)}$	0.1$^{(e)}$	0.32$^{(f)}$	0.013$^{(f)}$	0.075$^{(e)}$	0.27$^{(e)}$	0.13$^{(e)}$ 0.24$^{(f)}$
Conversion Time [ms]	0.0023	0.022	1	0.0133	300	839	59	0.01	1.3	765	33	μ = 0.67 σ = 0.081
Energy per Conversion [nJ]	0.67	3.4	93.6	9.92	0.23	8.9	11.56	0.94	12.8	4.9	0.46	μ = 1.06 σ = 0.127
R-FoM[(c)] [nJ·K2]	0.237	0.3	0.216	1.147	0.02	0.19	0.116	0.096	0.022	0.028	0.033	0.061
Supply sensitivity [°C/V]	43$^{(d)}$	34	-	13.6	8.4	3.8	13.7	2.4	5.76	2.8	16	8.21
Power [W]	288μ	154μ @27 °C	93.6μ	744μ	763p @27 °C	11n @25 °C	196n @30 °C	94μ	9.3μ	6.4n	14n @25 °C	1.57μ @25 °C

(a) Estimated area for non-linearity correction logic [9, 26]. (c) R-FoM = Energy/Conversion Œ Resolution^2. (e) Counter resolution. * External reference signal required.
(b) Relative Inaccuracy = (Max Inaccuracy Min Inaccuracy)/Temperature Range x 100. (d) Simulated result. (f) Noise-limited resolution.

Following a two-point calibration scheme utilizing 10 °C and 90 °C as temperature references, our sensor achieves an relative inaccuracy of 2.85% and a peak inaccuracy of approximately 1.4 °C. These values fall well within the stringent specifications demanded by multi-core systems [8, 21], affirming the robustness and accuracy of our sensor across the entire temperature range from 0 °C to 100 °C. Notably, these results are attained without the need for additional non-linearity correction logic, highlighting the inherent effectiveness of the calibration strategy.

The sensor further exhibits a noise-limited resolution of 0.24 °C and an average energy per conversion of merely 1.06 nJ with an average measured conversion time of 0.67ms across 20 samples. This combination of accuracy, resolution, and energy efficiency culminates in a competitive Resolution Figure-of-Merit (R-FoM), defined as $Energy/Conversion \times Resolution^2$ [28]. This is visually depicted in Figure 4.21, where the R-FoM/area trade-off for the compared de-

signs is illustrated. The reported results position our sensor in a favorable position, outperforming competitors in terms of both accuracy and energy efficiency. This underscores the overall excellence of our sensor design across critical performance metrics.

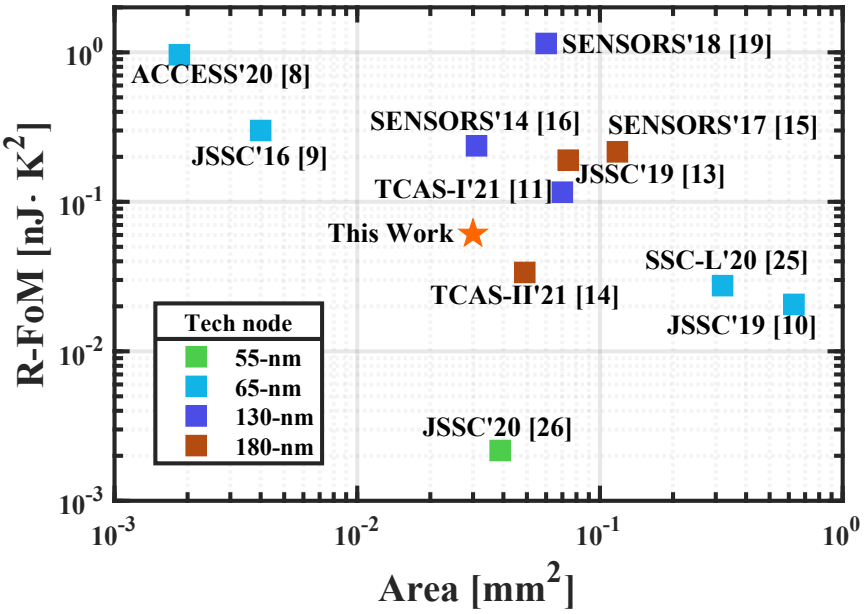

Figure 4.21: R-FOM vs silicon area.

4.5 Conclusion

This chapter introduces a fully-integrated CMOS temperature sensor designed for dense thermal monitoring in advanced SoC architectures. Leveraging a low-complexity circuit topology, the sensor offers a compact footprint, voltage scalability, low-power consumption, and high accuracy across a broad temperature range. Fabricated using a 180 nm CMOS standard technology, the sensor has went experimental characterization, showcasing competitive performance in comparison to state-of-the-art counterparts. The inherent features of our proposed sensor make it well-suited for integration into modern SoCs, addressing the increasingly critical need for efficient and accurate thermal monitoring in densely packed electronic systems.

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V. CONCLUSION AND FUTURE WORK

In this thesis, the design and testing of energy-efficient smart temperature sensors based on MOSFET devices was explored. The presented works targeted two main applications: IoT nodes such as the proposal introduced in Chapter III and Dynamic Thermal Management as the design presented in Chapter IV. Both temperature sensors accomplished competitive energy efficiency within their own design constraints, which are discussed in the following, among with recommendations for improvements.

The main characteristics from the ultralow voltage, ultralow power smart sensor presented in Chapter III can be summarized as follows.

- The ability to support a nominal V_{DD} of 350mV supply voltage to operate which is beneficial for low voltage IoT battery powered applications.
- Just $14\,\mathrm{nW}$ power consumption at $25\,^{\circ}\mathrm{C}$ with a consumed energy per conversion of $0.46\,\mathrm{nJ}$ and $33\,\mathrm{ms}$ of conversion time.
- A $0.27\,^{\circ}\mathrm{C}$ resolution over an operating temperature range of 0 – $100\,^{\circ}\mathrm{C}$ after a two-point calibration scheme at $20\,^{\circ}\mathrm{C}$ and $80\,^{\circ}\mathrm{C}$.
- Occupied silicon area of $0.049\,\mathrm{mm}^2$

In addition to these performance metrics the sensor achieved a R-FoM of $0.034\,\mathrm{nJ}\cdot K^2$ position it as a strong competitor given for energy-efficient sensors with a compact footprint at the expense of some resolution and conversion time, which would fit the constraints of IoT applications were such parameters are not critical and can afford a more relaxed behaviour. On the downside, the use of two-point calibration for each sample is still a requirement due

to the impact that process variations during lithography have on the proposed design. Voltage sensitivity is elevated since the design relies on subthreshold operation without the use of supply regulators.

The compact sensor for Dynamic Thermal Management (Chapter IV) possess a block diagram similar to the sensor presented in Chapter III, but with an extra addition as a form of voltage regulation and with a different design approach. Performance metrics of the compact sensor are listed below:

- A nominal V_{DD} of 0.6V with a full operating range 1.2V, from 0.6V to 1.8V.
- Compact footprint of 0.021 mm^2
- Noise-limited resolution of 0.24 $^\circ\mathrm{C}$
- Relative inaccuracy of -1.45 $^\circ\mathrm{C}$/1.4 $^\circ\mathrm{C}$ over an operating temperature range of 0 $^\circ\mathrm{C}$–100 $^\circ\mathrm{C}$, after two-point calibration.
- Energy per conversion of 1.06 nJ and a (mean) conversion time of 0.67ms

The most attractive characteristic of this sensor is the ability to operate at a wide voltage range, thanks to the native NMOS transistors stack used as a low-cost voltage regulator making the design attractive for advanced SoCs that require performing heavy dynamic voltage scaling, offering the possibility to work with similar levels of accuracy albeit using a different supply voltage setting, exhibiting a supply sensitivity of 0.56 $^\circ\mathrm{C}$/V at 30 $^\circ\mathrm{C}$.

Absolute inaccuracy sits at 2.8 $^\circ\mathrm{C}$, this value is appropriate for the demands of multi-core systems. Inaccuracy can be improved using some form of non linearity correction, which can be implemented on- or off-chip. During this thesis, the design route was to not make use of such techniques, nor the use of external signals as reference, this design preferences were adopted as

a measure to maintain the sensors cost as low as possible while being fully-integrated designs all together. The measured energy efficiency was of $0.061\,\mathrm{nJ} \cdot K^2$, a competitive value given the low area occupancy and the wide operating supply voltage range.

As discussed in Chapter 2.5 and showed in Table 4.1, MOSFET-based temperature sensors usually require a two-point calibration scheme to reach acceptable levels of accuracy. During the work in this thesis, the same calibration strategy was used with both sensors architecture (two-point calibration scheme). In both sensors a 1-point calibration technique was not feasible, this is due to the missing correlation between the slope of the temperature response and one of the magnitudes, for example, an oscillation frequency. If any correlation could be found, at least in simulations, since the frequency information was not available after tape-out, an expression could be developed in the form of slope=f(frequency) to obtain this parameter, then a 1-point calibration could have been performed. It has been shown before as well that some works that employ calibration on a single temperature usually exhibit larger power consumption that would eventually have a negative impact on battery-powered devices. Therefore, an interesting solution from the cost and time point of view would be to explore a temperature sensing architecture that requires a single temperature calibration to give competitive accuracy and energy efficiency while maintaining low voltage operation.

Another interesting proposal to improve the presented sensors design is to have a built-in solution where there is no need of separate Temperature to Current- and Current to Frecuency converters (TCCs and CFCs, respectively) but to have the sensing devices directly feeding CFCs to save space and avoid mirroring errors induced by mismatch.

Finally, the presence of FinFet technology in most modern System-On-Chips make an interesting appeal to develop integrated temperature sensors. Posing a challenge mainly at the optimization phase due to the discrete nature of device sizing.

VI. LIST OF PUBLICATIONS

[1] **B. Zambrano**, E. Garzón, S. Strangio, G. Iannaccone and M. Lanuzza, "A 0.6V-1.8V Compact Temperature Sensor With 0.24 $^{\circ}\mathrm{C}$ Resolution, $\pm$1.4 $^{\circ}\mathrm{C}$ Inaccuracy and 1.06 nJ per Conversion," in IEEE Sensors Journal, vol. 22, no. 12, pp. 11480-11488, June 15, 2022, doi: 10.1109/JSEN.2022.3171106.

[2] **B. Zambrano**, S. Strangio, T. Rizzo, E. Garzón, M. Lanuzza and G. Iannaccone, "All-Analog Silicon Integration of Image Sensor and Neural Computing Engine for Image Classification," in IEEE Access, vol. 10, pp. 94417-94430, 2022, doi: 10.1109/ACCESS.2022.3203394.

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[4] E. Garzón, **B. Zambrano**, T. Moposita, R. Taco, L. -M. Prócel and L. Trojman, "Reconfigurable CMOS/STT-MTJ Non-Volatile Circuit for Logic-in-Memory Applications," 2020 IEEE 11th Latin American Symposium on Circuits & Systems (LASCAS), San Jose, Costa Rica, 2020, pp. 1-4, doi: 10.1109/LASCAS45839.2020.9069027.