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An Analog/Mixed-Signal SoC-Package Co-Design Methodology for Early Stage Signal Integrity Assessment Exploiting the Potential of Machine Learning Models

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UNIVERSITY OF CALABRIA
Department of Computer Science, Modeling, Electronics and Systems Engineering

DISSERTATION

An Analog/Mixed-Signal SoC-Package Co-Design Methodology for Early Stage Signal Integrity Assessment Exploiting the Potential of Machine Learning Models

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I would like to dedicate this thesis to my Family

Author's Short Bio

Francesco Settino received the M.Sc. degree in electronic engineering (cum laude), from the University of Calabria, Cosenza, Italy, in 2015, where he is currently pursuing the Ph.D. degree in Information and Communication Technologies. He has been with the University of Udine as a contract researcher (April 2016 - March 2017), working on the evaluation of the performance of Tunnel FET for analog applications.

Since April 2017 he is with Infineon Technologies AG, Villach, Austria, working on his Ph.D. thesis with main focus on chip-package-board co-design methodology to address "Signal Integrity" challenges in complex analog/mixed-signal SoC-package design for automotive applications.

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Abstract

The development of new generation System-on-Chip (SoC) is mainly driven by the demand of an ever increasing number of functionalities at reduced cost and time-to-market. This is enabled by re-using specialized functional blocks, generally referred as intellectual property (IP) blocks. However, each block (analog, digital, analog mixed-signal) is typically designed and optimized independently either in-house or by a third-party vendor. This leads to an increased design complexity, making the integration of the analog mixed-signal (AMS) blocks very challenging. As the switching behavior ($\mathrm{d}i/\mathrm{d}t$ and $\mathrm{d}v/\mathrm{d}t$) of the chip signals increases due to higher clock frequency, the package and board interconnects start to contribute significantly to the overall system-level performance. Signal integrity is a main issue in package designs due to the parasitic effects of capacitive/inductive coupling between potential aggressor and victim signals. In general, fast switching signals can induce unwanted disturbances into sensitive signals due to crosstalk effects even via off-chip interconnects, which may degrade significantly the overall system-level performance.

A SoC for automotive applications typically requires several high accuracy analog-to-digital converters (ADCs), which are key blocks to sense and process the external inputs in order to quickly react at system-level (especially for safety requirements). However, those ADCs need to be integrated in a complex environment that comprises many different IP blocks (e.g. power converter or high-speed interfaces) at high switching frequency that can act as potential aggressors. Hence, next generation of SoC will face a significantly higher number of aggressor-victim couples. On the other hand, more accurate mixed-signal circuitries such as voltage monitoring will be required especially for advanced driver assistance systems (ADAS) application due to safety requirements.

Reliable and accurate prediction of the system-level behavior by chip-package-board co-design is essential to achieve “right first time” solutions. A machine learning approach can save significant time considering the main challenges in performing system-level simulations, mainly related to circuit complexity and convergence issue due to the integration of the package model (typically S-parameter data). This research work focuses on the development of a methodology exploiting machine learning algorithm to enable optimized SoC-Package co-design right from the early stage of the development cycle. The main target is to detect potential specification violation issues at system-level that may occur due to signal integrity challenge at package-level, providing guidelines for package design, and a quick feedback for the chip design development towards the optimization of the overall chip-package-board system, optimizing development cycles and time-to-market for competitive products.

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Chapter 1

Introduction: What? Why? How?

Semiconductor content in the automotive market has grown significantly in recent years due to the increasing demand for safety-critical applications to support electrical mobility, autonomous driving and advanced connectivity for next generation vehicles. In a typical application, such as the advanced driver assistance systems (ADAS), many sensors are combined with a microcontroller (μC) in order to fulfill the system-level performance requirements. The μC is a System-on-Chip (SoC) design, which includes many digital, analog and mixed-signal (AMS) modules, generally referred to as intellectual property (IP) blocks. In general, heterogeneous blocks such as connectivity module, analog-to-digital converter (ADC), and embedded power converter module are co-integrated on the same chip. The development of an automotive SoC design has to face different challenges both from chip and package design perspective in order to find an optimal trade-off between development cost, cost of the final product and time-to-market requirements. In addition, next generation of SoC design, driven by the demand of increasing performance and functionality, will require package design with higher electrical performance, which contributes significantly to the cost of the final product (i.e. comparable to the cost of silicon area). Therefore, the package design starts to play a key role in terms of cost and performance of the final product. In this context a fast and reliable chip-package co-design methodology to evaluate the system-level performance and optimize the design as early as possible during the development cycle is the key enabler for achieving "*right first time solutions*".

1.1 AMS SoC-package design development cycle

The development of modern automotive SoCs requires the integration of more and more CPUs, DSPs, memories, and power management IP blocks, which have to be co-integrated with many high-performance analog and mixed-signals blocks [1]. The increasing number of AMS blocks that need to be co-integrated on one hand and the increasing design complexity on the other hand lead to new challenges on both chip and package design, which may slow down the development cycle. A condensed overview of a typical SoC-package design development cycle, is reported in Figure 1.1.

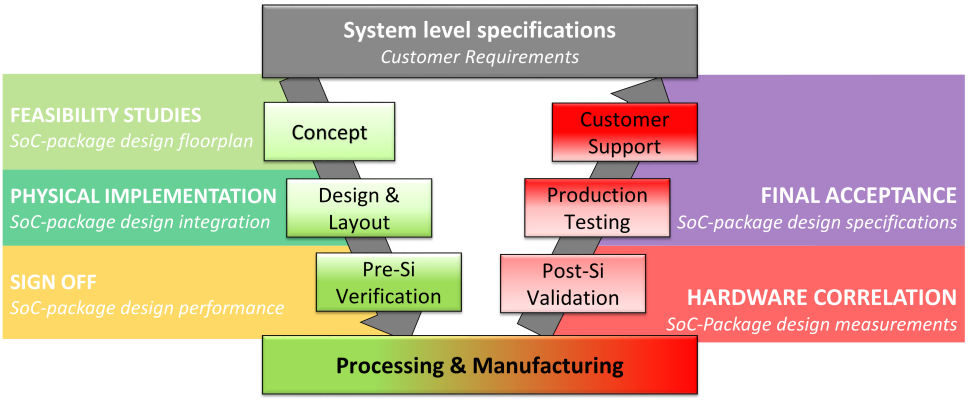

Figure 1.1 Overview of the typical SoC-package design development cycle.

In order to meet the time-to-market requirements, SoC designs rely on IP-block reuse [2], which are typically developed either in-house from different design teams or by a 3rd party company. This approach allows to reduce the development cost and time at the expense of an increasing integration complexity. A hierarchical top-down approach is typically implemented to reduce complexity of the design problem enabling fast engineering change order (ECO) loops between the different development phases. In the past, package design frequently was not synchronized with chip design, but that approach cannot be continued with most recent challenges. The die data are exchanged between different domains via AIF file format, which is a simple ASCII file describing the die for purposes of package design [3]. In addition, the board design is driven by the requirements of customers, which limits

any freedom to change the package pin-out specifications (i.e. signal and power supply assignment) due to backward compatibility reasons. Consequently, the chip-package-board design system results to be developed independently as sketched in Figure 1.2.

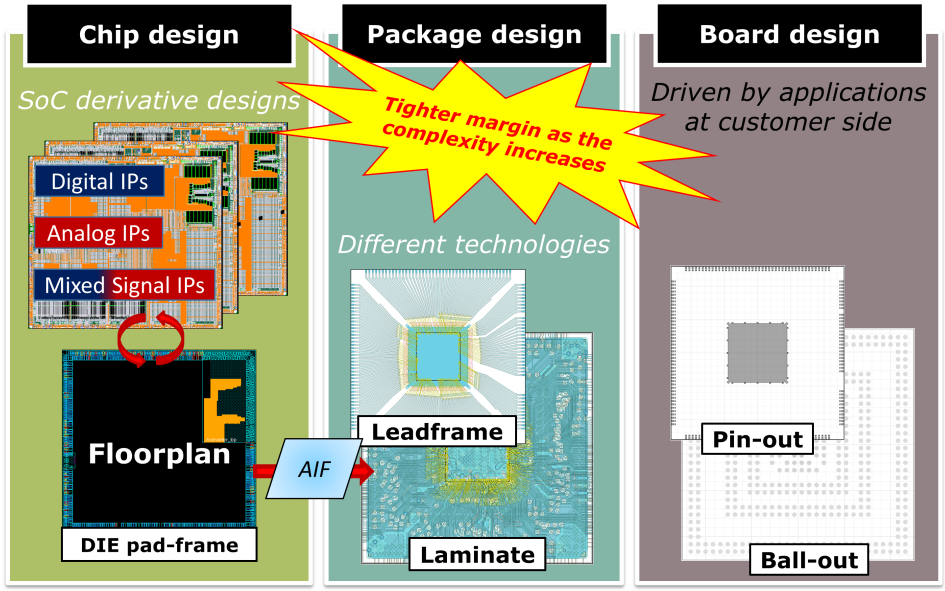

Figure 1.2 Overview of the traditional chip/package/board design development.

Meeting the specification requirements at block-level and SoC-level usually ensures successful system-level performance. An issue detected after the fabrication process may jeopardize the final acceptance of the SoC-package performance by the customer, leading to delays in time-to-market. Therefore, modern AMS SoC-package design demands specific co-design and co-verification methodologies [4] for early detection of potential specification violation issues during the development cycle.

1.1.1 SoC-Package technology trend

Driven by the advances in chip technology node, the SoC technologies have the potential to integrate an ever increasing number of functionalities [5] in order to fulfill growing requirements in automotive applications.

The increasing complexity and high performance requirements of an automotive SoC are also shaping the package technology trend. An overview of both chip and package technology trend is reported in Figure 1.3.

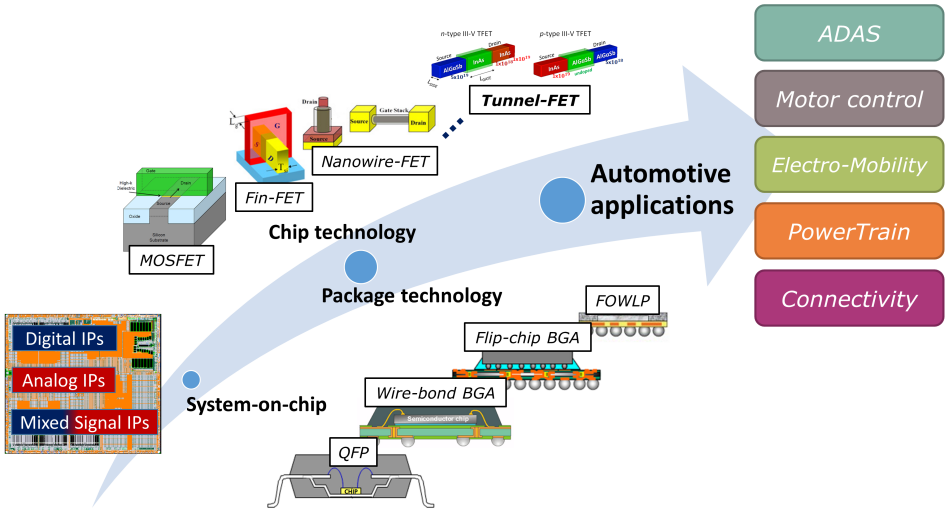

Figure 1.3 Chip and package technology trend for automotive applications.

Since its first demonstration in 1959 the metal oxide semiconductor (MOS) field effect transistor (FET) [6] has become by far the most widely used technology in modern integrated circuits (ICs). The MOSFET is essentially a 4 terminals device which uses the voltage applied to the "gate" terminal to generate an electric field that control the current flow through the channel between the "drain" and "source" terminal, while the "bulk" terminal can be seen as additional control terminal with lower control compared to the gate.

For more than 50 years now, following Moore´s law [7] (i.e. the number of transistors in an IC will double every 18 months), scaling of MOSFET technology allowed to achieve an increased integration density and faster switching speed at reduced cost and power consumption. However, short channel effects start to prevent the gate to have full control of the channel in a planar MOSFET implementation, limiting its electrical performance. Nowadays, FinFET architecture has already replaced the planar one for technology node beyond 22 nm, while gate-all-around FET technology (nanowire and nanosheet FET) are planned to extend Moore´s

law to overcome various limitation toward the 5 - 3 nm node. Beyond that, it´s difficult to anticipate which new technology will replace or complement the MOSFET, although an alternative approach could be the integration of more devices in advanced package solutions, also called hybrid scaling or heterogeneous integration, which is already visible in today´s high-end consumer products. Research works have investigated different options such as the Tunnel FET (TFET) technology, which has been identified as a potential solution amongst many others for low-voltage and low-power applications [8]. In this context, several research activities have been carried out within this thesis work investigating the potential and limitations of TFET compared to FinFET technology for digital and analog-mixed signal circuit designs [9], [10], [11], [12].

In the realm of the automotive applications both mature and advanced technology node would be required for next generation of autonomous vehicles. On one hand the surrounding sensors and control unit demands for more mature and robust technology processes because of safety requirements, while on the other hand the artificial intelligence (AI) computing power required for post-processing of sensors data in real-time to enable autonomous driving demands for high-performance technology. The technology node scaling may impact the SoC development in terms of:

- *IP reusability*, because different technology nodes may lead some circuits to behave differently requiring the implementation of a new circuit topology in order to meet the IP block performance specification.
- *IP integration scenario*, because the integration of more complex and faster IP blocks may lead to an intrinsically noisy environment, affecting the performance of all other sensitive AMS IPs.

Overall this leads to an increased SoC design complexity from one generation to another and even from one derivative design to another, impacting also the package development. The main target for package development is to lower cost, increase density, and improve the performance to fulfill the system level requirements, while keeping or improving the reliability. Currently the package portfolio for the automotive μC includes lead frame package technology such as quad flat package (QFP), and wire-bond ball grid array (BGA) package. The main differences are highlighted in Figure 1.4.

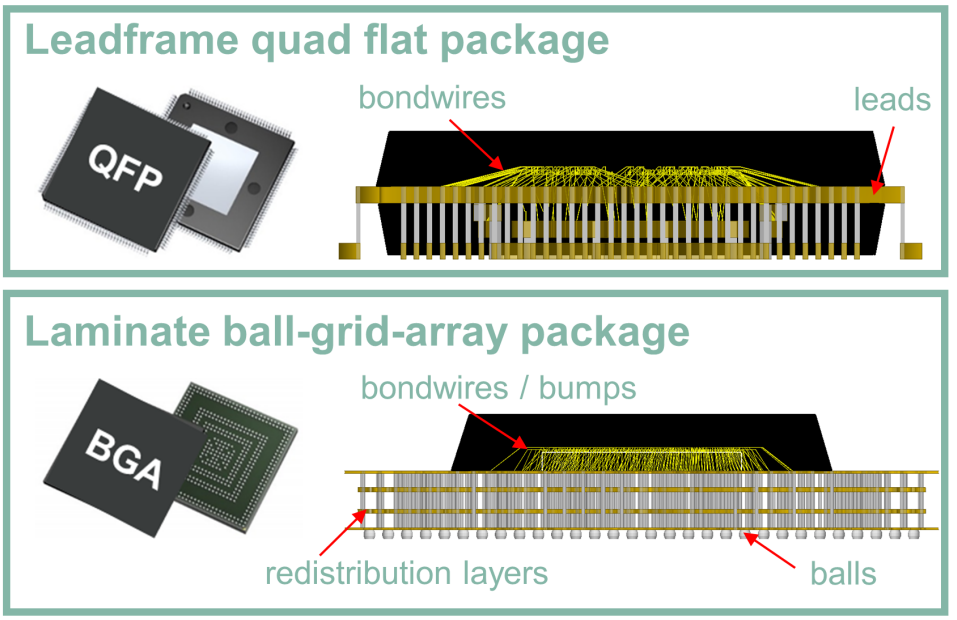

Figure 1.4 Comparison between QFP and wire-bond BGA packages.

QFP packages are exploited for low end application and constitute the largest type of packaging because of their high reliability. However, due to electrical limitation of such a package technology, for high-end performance the wire-bond BGA packages are employed. To address the increasing complexity and performance requirement of next generation of μC, the package technology is moving to high performance flip-chip BGA and advanced fan-out wafer-level packages (FOWLP) [13]. The key advantage of flip-chip technology compared to wire-bond technology is the possibility to locate the bumps on the die side close to the sensitive IP blocks, improving the power integrity and signal integrity performance of the SoC-package design. However, package design cost starts to contribute significantly to the overall cost of the product [14].

1.1.2 Bridging the gap between AMS SoC and package development

The increasing complexity of the new generation of automotive SoC on one hand and the advances in technology node (i.e. increasing switching speed of the signals)

combined with the package interconnects (i.e. parasitics behavior) on the other hand, results in potential rise of Signal Integrity (SI) and Power Integrity (PI) challenges [15]. Those problems may lead to a package re-design due to a specification violation issue detected too late during the development cycle. A traditional approach where the chip and package design are developed independently is no longer sufficient to guarantee the system-level performance requirements. Therefore, the role of the chip-package co-design is expected to be increasingly crucial on next generation of SoC design in order to deal with the increasing complexity and reduced time-to-market [16], [17]. Several feedback loops between chip and package development are typically required in order to optimize the SoC-package design, reducing cost and time-to-market. A sketch is reported in Figure 1.5.

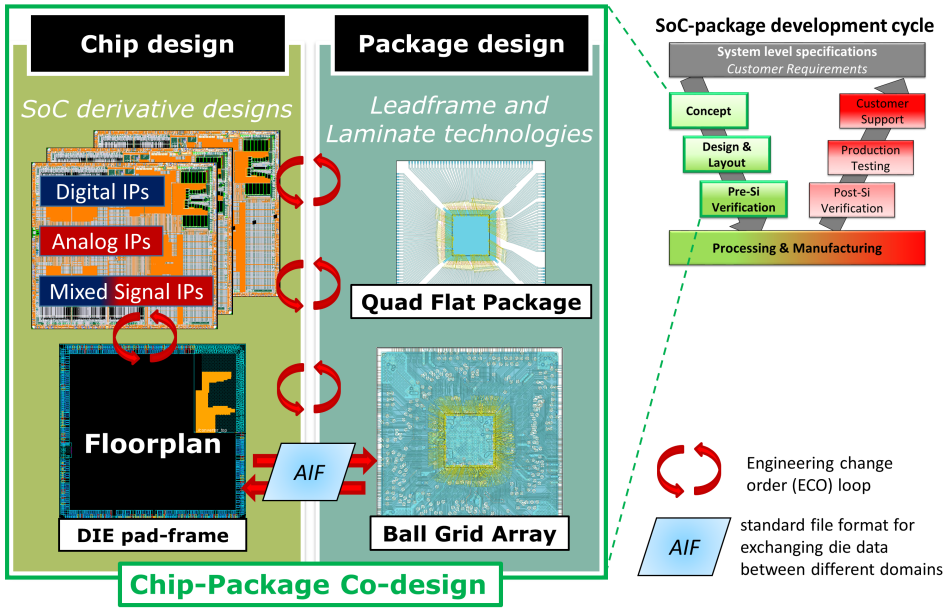

Figure 1.5 Overview of a typical chip-package co-design methodology.

Typical chip-package co-design methodologies address power integrity issue (i.e. related to the power delivery network design) and signal integrity issue (i.e. related to the quality of the signal) separately, while a more comprehensive power aware signal integrity analysis is required to investigate potential noise issue affecting the

performance of sensitive AMS IP blocks. However, bridging the gap between chip development and package development with effective chip-package co-design is not only linked to technical challenges. Also the development of necessary skills and the required collaboration among design teams have an impact on performing effective concurrent design activity. As the package design starts to impact significantly the system-level performance, accurate early stage prediction via co-design methodology of the SoC-package design is essential to drive the physical-design planning (e.g. IP block placement, pin assignment), in order to minimize the number of ECOs loops to optimize the chip-package design while keeping package cost low [18].

1.2 Organization of the dissertation

The dissertation starts with a review of the chip-package co-design methodology in Chapter II, highlighting the gap between the well-established early stage signal integrity and power integrity analysis for the high-speed digital design development and optimization compared to the few works reported on the co-simulation and co-analysis for complex analog/mixed-signal design. In Chapter III, a SoC-package co-simulation methodology has been developed in order to predict the RMS-noise behavior of the ADC analog channels, which experience noise coupling at package-level from the DC/DC converter. In addition, a step-by-step chip-package co-design methodology is presented in Chapter IV to mitigate potential coupling path and optimize the package design. Chapter V reviews the basics of a machine learning approach and its main applications to electronic circuit design and optimization. In particular, the potential and limitations are discussed with respect to chip-package co-design activities. A machine learning approach based on support vector machine (SVM) is developed in Chapter VI in order to deal with the high volume of package derivatives and complexity of the simulation, showing the potential of such an approach for early stage SoC-package performance prediction. Finally, future research perspective on the extension of such a machine learning based chip-package co-design methodology is discussed along with the main conclusions.

Chapter 2

Signal Integrity analysis in AMS SoC-Package design

Signal integrity (SI) refers to two main aspects of a signal: the timing and the quality as it travels through the SoC-package physical design. As the complexity of the automotive SoC increased and the clock speed became faster with the technology development, the electrical requirements posed on the package design started to be very challenging. Therefore, co-simulation methodologies are required to perform accurate and reliable SI analysis of the SoC-package system. In this chapter an overview of typical chip-package co-simulation and co-analysis are discussed, highlighting the main challenges when analog/mixed-signal circuits are considered, compared to the well-established approach for high-speed interface design. Furthermore, the different modeling approaches for package-board interconnect design are discussed highlighting the main challenges, which arise from model extraction and integration in a SPICE-like circuit simulator.

2.1 Overview of typical co-simulation analysis

SI problems mainly arises from electromagnetic (EM) fields problems, such as reflection (interconnect discontinuities), crosstalk (electromagnetic coupling between interconnects), or power/ground bounce (parasitic elements in the power delivery network) [19].

Understanding these problems from EM perspective is essential to derive an effective solution as early as possible during the design cycle, reducing development time and cost. SI problems may occur at any level of the SoC-package physical design as well as on the printed circuit board (PCB). A sketch of a typical automotive package-board interconnect system is shown in Figure 2.1

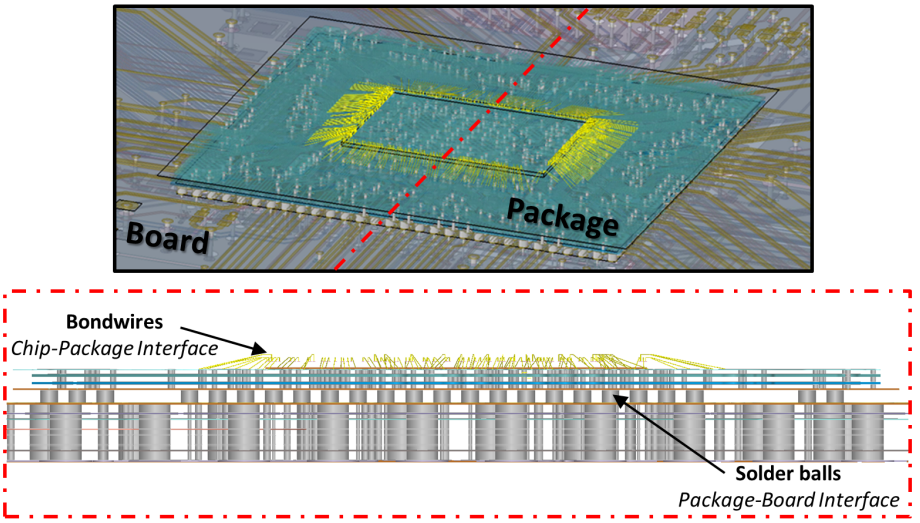

Figure 2.1 3D view and cross-section of typical package-board interconnects.

Such a complex system consists of bondwires (used at the chip-package interface), traces (possibly routed over the corresponding power/ground planes), vias (used to route the traces on different layers), and solder balls (used at the package/board interface). SI issues are directly related to the rise time of the signal, which is becoming shorter as the clock speed increases with the advances in technology node (in most high-speed digital systems, typical rise/fall times are around 10% of the clock period). Therefore, SI challenges typically arise from a fast switching signal which propagates through the package-board interconnect system affecting the quality of the signal itself or of a sensitive signal routed nearby.

In the past package designs were mainly designed for mechanical stress from soldering and application over lifetime, with less focus on the intrinsic electrical performance. Signal integrity issues did not always matter, but now are gaining

much more importance and becoming crucial for new generation of automotive SoC-package design, which integrates several high-speed design (such as DDR, RGMII, PCIe interfaces) as well as an increased content of accurate AMS blocks (such as ADC and power management system).

2.1.1 Co-design methodology for power aware SI analysis

Nowadays, SI for high-speed digital designs is considered in the early stage of the development to define guidelines and constraints for physical design implementation, such as package types, net topology, pins and balls assignment. Chip-package-board co-simulation methodology has to be considered to accurately assess the SI performance (i.e. amount of reflected noise, ringing, crosstalk and ground bounce) and to ensure the success of the high-speed digital design. A typical co-simulation analysis, sketched in Figure 2.2, involves the accurate modeling of the chip behavior along with an electrical model of the chip-package-board interconnect design.

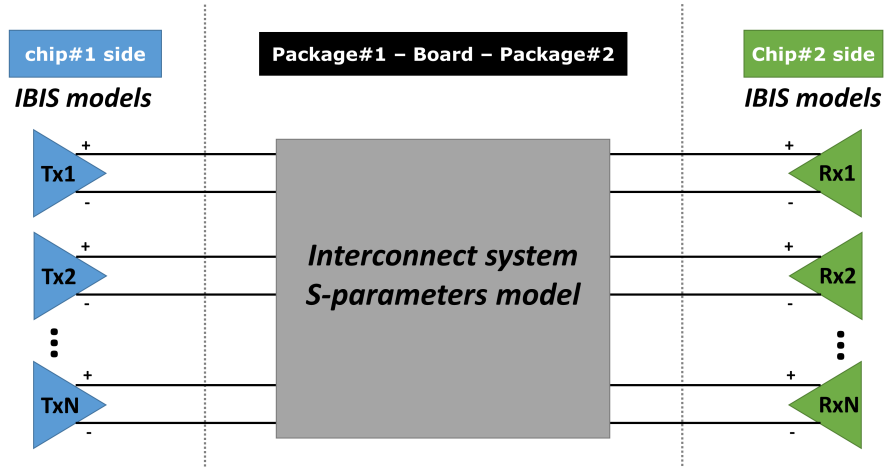

Figure 2.2 Sketch of a typical chip-package-board co-simulation for high-speed design.

The traditional approach involves the use of transistor level models, however, the SI analysis requires the simulation of many nets and has to be fast enough to perform what-if analysis, therefore the full-transistor model of a transmitter (Tx) / receiver (Rx) is typically replaced with IBIS models [20]. The Input/Output Buffer information specification (IBIS) is a standard approach to accurately model the

behavior of a driver/receiver circuit. Those models avoid to disclose any proprietary information and are capable of maintaining the required accuracy and speed for signal integrity analysis. Behavioral modeling techniques have also been developed in many research works to model non-linear digital I/O driver/receiver [21], [22], [23], which turned out to be a more accurate and efficient approach compared to standard IBIS models. Furthermore, as the voltage margins decrease due to technology scaling, also the noise on the power delivery network (PDN) starts to contribute significantly to the quality of the signal. As discussed in [24] the power/ground interconnects may act as an additional noise source instead of an effective shield if not properly designed. In order to perform power aware SI analysis the IBIS v5.0 can be used as valid alternative to full transistor-level models [25].

Many research works have focused on chip-package-board co-simulations and co-analysis methodology to address signal integrity (SI) and power integrity (PI) performance in high-speed system design, such as DDR memory module [26], [27], [28], [29] and high-speed serial links [30], [31], [32], [33], [34]. These works investigated the optimization of the high-speed interface itself, while only few reported works have investigated co-integration issue (i.e. SI issues amongst different interfaces, one acting as aggressor while the other one is a victim). For example, the co-integration and co-existence of a high-speed module (HDMI module, acting as aggressor) and a RF wireless system (WiFi module, acting as victim) is investigated in [35]. While [36] addressed the coupling from a DC-DC converter (acting as aggressor) to nearby high-speed signals (acting as the victims). However, only few works have been devoted to develop fast and reliable co-simulation methodology for sensitive AMS blocks. AMS blocks, acting as victim, may experience signal integrity issue due to the noise coupled from fast switching blocks which act as aggressor. As the complexity of an automotive SoC-package design increases and the advances in technology node lead to an increased switching speed, the number of aggressor-victim pairs is expected to grow significantly. This leads to increasingly complex physical implementation problems. Therefore, signal integrity analysis which is critical for any high-speed digital design, would be required also to ensure the successful integration of analog/mixed-signal design. In [37] a package-board co-simulation methodology is developed to model the effect of magnetic field from a wireless power transfer (WPT) system on the ADC performance. While [38] investigates the degradation in

ADC performance due to the coupled noise via the power delivery network (PDN) of the chip-board interconnect system.

2.2 Signal integrity: crosstalk

Crosstalk refers to the electromagnetic (EM) coupling between adjacent interconnect lines (including both the signal and its return path). This can cause noise appearing on a sensitive line, which acts as a victim due to the switching activities on the other line which acts as the aggressor. The coupled noise may be generated either from a coupling between signal lines as well as between power supply and signal lines. The amount of crosstalk can be quantified as the ratio of the coupled noise level appearing on the victim line and the aggressor voltage level, expressed in percentage. Typically, high-speed digital application may tolerate crosstalk level up to 5%, while for sensitive analog application a much lower crosstalk level may be required (as low as 0.01%). For example, for a 12 bit ADC it is required to have an error of less than about 0.5 LSB, which means that the coupled noise should be less than approximately 0.6 mV (i.e. considering that 1 LSB corresponds to about 1.22 mV). Therefore, in a scenario where an aggressor signal of 5 V couples to an ADC analog input, the amount of crosstalk should not exceed roughly 0.012%.

For a generic aggressor-victim pair, the severity of the crosstalk noise is essentially driven by the combination of the following elements:

- the *aggressor switching activity strength* determined by the signal rise time
- the *victim noise sensitivity profile* at the input or power path
- the *interconnect coupling path* due to mutual capacitance and inductance

Crosstalk may take place at any level inside the whole interconnect path from the chip to the board. In particular, for interconnects behaving as uniform transmission lines (i.e. interconnects routed over a wide uniform plane which provides the return path), as in most board designs, the amount of capacitive and inductive coupling is almost the same. This scenario results to be the best to keep the amount of crosstalk as low as possible. While for interconnects behaving as non-uniform transmission lines, as in package designs (i.e. the return path is different from a wide uniform

plane), the inductive coupling dominates the capacitive one, which leads to an increased crosstalk noise [39]. In this scenario the crosstalk noise is dominated by the inductively coupled currents and, therefore, is more commonly referred to as switching noise or di/dt noise. Furthermore, even if only one aggressor line may not be relevant for crosstalk, the simultaneous switching of several lines may generate a significant crosstalk noise, referred to as simultaneous switching noise (SSN).

2.2.1 Understanding the coupling path

Understanding the coupling mechanism at the origin of the crosstalk noise is essential to optimize the physical interconnect design and to mitigate the problem. As the aggressor signal travels along the interconnect, it generates electric-field lines between the signal and its return path, as well as magnetic-field lines around the signal and its return path. The electro-magnetic (EM) field lines are not confined in the space between the signal and its return path, generating fringe fields into the surrounding environment. A victim signal and its return path, which is routed in a region where those fringe fields are still effective, may pick up noise when the aggressor signal is switching. The transients of voltage and current in the aggressor line induces a current flow through the changing electric and magnetic fields. This coupling mechanism can be modeled at first level approximation by lumped elements as sketched in Figure 2.3.

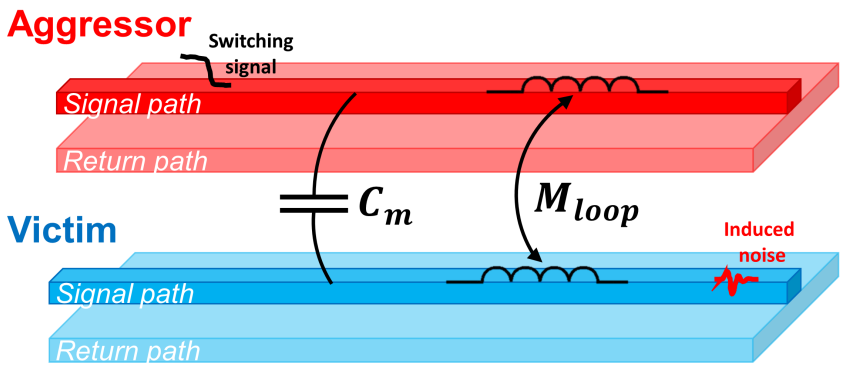

Figure 2.3 Sketch of a generic aggressor-victim coupling mechanisms.

Therefore, a combination of capacitive coupling (i.e. mutual capacitance, C_m) and inductive coupling (i.e. loop mutual inductance, M_{loop}) exists between any aggressor-victim line pair, which constitutes the path for the unwanted crosstalk noise. In particular, a voltage change in the aggressor line induces a current noise into the victim line, which can be approximated as:

$$I_{\text{noise}} = C_m \frac{dV_A}{dt} = C_m \frac{I_A \cdot Z_0}{t_{\text{rise}}}$$

where:

– C_m is the mutual capacitance between the aggressor and victim lines

– V_A is the signal voltage in the aggressor line

– I_A is the signal current in the aggressor line

– I_A is the signal current in the aggressor line

– t_{rise} is the rise time of the aggressor signal voltage

– Z_0 is the typical impedance seen by the signal in the aggressor and victim lines

In a similar way, a current change in the aggressor line induces a voltage noise into the victim line, which can be approximated as:

$$V_{\text{noise}} = M_{\text{loop}} \frac{dI_A}{dt} = M_{\text{loop}} \frac{V_A}{t_{\text{rise}} \cdot Z_0}$$

where:

– M_{loop} is the mutual loop inductance between the aggressor and victim loops

– I_A is the signal current in the aggressor line

– V_A is the signal voltage in the aggressor line

– t_{rise} is the rise time of the aggressor signal current

– Z_0 is the typical impedance seen by the signal in the aggressor and victim loops

In practice, the only terms which depend on the chosen package design technology are the mutual capacitance and the loop mutual inductance between interconnects. Considering the package interconnects, where the return path is not a wide uniform plane, the crosstalk noise will be dominated by the loop mutual inductance. In particular, once the switching noise margin (V_{noise}/V_A) is specified, the maximum allowable loop mutual inductance is given by:

$$M_{\text{loop}} = \frac{V_{\text{noise}}}{V_A}(t_{\text{rise}} \cdot Z_0)$$

Considering the example of a 5 V aggressor signal coupling into a sensitive 12 bit ADC input, the crosstalk noise margin resulted to be 0.012%. Now, assuming an aggressor current rise time of about 1 ns and a typical impedance of 50 Ω, the maximum allowable loop mutual inductance results to be 6 pH.

2.2.2 Common mitigation techniques

In general, if the coupled noise exceed the noise margin defined for the victim circuit, mitigation techniques need to be applied, such as:

1. *Reduce the aggressor strength* by implementing a smoother transition during the switching activity.

2. *Improve the victim noise sensitivity* by implementing a more robust circuit topology to increase the margin.

3. *Change the timing* by synchronizing the aggressor and victim circuits such that the aggressor signal switches when the victim is less sensitive to noise.

4. *Reduce the number of simultaneous switching aggressors* by introducing some skew between the signals, which translates a single crosstalk noise spike into a sequence of smaller spikes.

5. *Improve the coupling path* by implementing an optimal physical design for the aggressor and victim interconnects loop.

However, it should be considered that adjusting the aggressor switching behavior or the victim sensitive profile may not be an option due to the high reuse of IP

blocks in a SoC design or the specification requirements dictated by the system-level application. Synchronization may be a valid option since crosstalk only happens within a time frame defined by the switching period of the aggressor signals and its rise/fall time. However, it may be very challenging from physical implementation point of view to be deployed at SoC-level. Furthermore, the additional synchronization circuitry may impact the performance of the IP block that is receiving the synchronization signal.

Therefore, in most cases the only option amongst the reported mitigation techniques is to try to make the aggressor signal not effective by reducing the coupling path to the victim line. The amount of coupling between interconnect is primarily related to the spacing between lines and how long they run in parallel to each other. In particular, capacitive coupling is a short range effect which drops off quickly with the distance between interconnects. Therefore the best way to reduce it is by increasing the separation between aggressor and victim interconnects or adding a ground shielding line in between. Shielding techniques are widely used to mitigate crosstalk issue and can be summarized in two main categories: passive shielding (i.e. power/ground lines are routed between critical interconnects, acting as a shield) [40], [41] or active shielding techniques (i.e. dedicated switching line, instead of power/ground lines are used as shield) [42], [43]. Although the latter show better performance in shielding effectiveness, they introduce additional area and power consumption.

Instead, inductive coupling is a long-distance effect which involves the current loops created by the signals and their return paths. In this case one of the following approaches may be used to reduce the loop mutual inductance:

- *reduce the length of the aggressor and victim loops*, which translates in making the package interconnects as short as possible.

- *increase the spacing between the aggressor and victim loops*, which is somewhat limited by the chosen package technology.

- *keep the signal closer to its return path for both the aggressor and victim loops*, which decreases the loop self-inductance of both loops as well as the loop mutual inductance between them.

2.3 Electrical modeling of package design

Modern SoC-package designs are complex systems which require EM simulators to evaluate the impact of the package parasitics on system-level performance in order to meet the time-to-market requirements. Package elements such as bond-wires, metal traces routing, via transition, and power/ground planes need to be accurately modeled to consider all the EM effects that may lead to SI problems. Nowadays, various EM simulators are available to solve Maxwell´s equations, depending on the most suitable approach for the type of problem under investigation.

Common methods are:

- *Finite Element Method (FEM)*, which is the most popular numerical method based on solving the partial differential equation formulation (a volume mesh is typically required). The main advantages over others methods is the ability to model structures by using both coarse and fine mesh depending on the granularity which is locally required.

- *Finite Difference Time Domain (FDTD)*, which is the most popular technique to solve Maxwell´s equations with time-dependent boundary conditions. The main advantage of this method is the possibility to efficiently visualize the electric and magnetic fields everywhere in the computational domain as they evolve in time.

- *Boundary Element Method (BEM)*, also called Method of Moment (MoM), which is the most popular frequency-domain technique based on the integral equation formulation (a surface mesh is applied). The main advantage of this method is at solving open radiation problems.

A comprehensive overview of the EM simulators available on the market grouped by type, cost and employed numerical techniques, is available in [44].

2.3.1 Modeling approach: lumped vs. distributed circuit models

The choice of the modeling approach to be used is basically dictated by the package design structure and the frequency of the signals involved in the specific application.

To determine whether a lumped or distributed circuit model is necessary, as a rule of thumb, the physical length of the package interconnects has to be compared with the electrical length, which is expressed in terms of wavelength (λ). For a digital signal λ is related to the highest frequency content of the signal and therefore can be related to its rise time. In particular, it can be shown that, for a realistic waveform, most of the energy is contained inside the spectrum from DC to the knee frequency [45], estimated as:

$$f_{\text{knee}} \approx \frac{0.5}{t_{\text{rise}}}$$

where t_{rise} is the rise time of the signal (defined from the 10% to the 90% point).

In particular, at the knee frequency the spectrum of the waveform results to be 6.8 dB below the -20 dB/dec straight slope. Instead, in [19] the relationship between the rise time and the bandwidth of an ideal square wave is approximated as:

$$\text{BW} \approx \frac{0.35}{t_{\text{rise}}}$$

In this case the spectrum of the signal is considered 3dB higher (i.e. 3.8 dB below the straight slope). Both rule of thumbs can be used equivalently as a first order estimation of the maximum frequency content of a signal.

Instead, the wavelength can be computed from the highest frequency content of the signal, as:

$$\lambda = \frac{c_0}{f \cdot \sqrt{\varepsilon_r}}$$

where:

- c_0 is the speed of light in empty space (about 3×10^8 m/s)
- f is the frequency of the signal
- ε_r is the relative permittivity of the considered dielectric material

If the physical dimensions of the package interconnects are much lower than 1/10th of the wavelength, a lumped modeling approach can be used, otherwise a distributed modeling approach is required.

In a lumped model, the voltage across both ends of the package interconnect and the current through it are assumed to change instantaneously and the travel time is neglected (quasi-static approximation). Instead, in a distributed model the current and voltage vary along the conductor (i.e. transmission line effect have to be considered). A widely used approach consists in using n-section lumped model approximation. In this configuration, the capacitance and loop inductance as well as their mutual contributions are distributed uniformly and expressed for unit length (assuming a uniform transmission line scenario). As a rule of thumb, for a good approximation, one section is required for every 1/10th wavelength of the signal [19]. However, for higher frequencies where voltages and currents are difficult to be defined and the signal is best represented by a traveling wave, the distributed modeling approach may be not accurate enough and a scattering parameters model is required.

2.3.2 S-parameters modeling

Scattering parameters, commonly referred to as S-parameters, are used to describe the electrical behavior of any linear, passive electrical network [46]. Different from other type of parameters like Y-parameters, Z-parameters or ABCD-parameters, which exploit open or short circuit conditions, the S-parameters rely on load matching to characterize the linear network, which is considered as a “black box”. S-parameters vary with frequency and are represented as a square matrix of complex numbers (commonly referred to as S-matrix), where the frequency is specified for each element in addition to the characteristic impedance (for example 50 ohm). In general, they can be applied at any frequency, but they are commonly used for characterization of electrical network operating in the radio frequency (RF) range (from around 20 kHz to around 300 GHz).

An electrical network characterized by S-parameters may have an arbitrary number of ports, where each port is constituted of two terminals (one serves as reference) under the requirements that the current leaving one terminal is equal to the one entering the other terminal. Therefore, the S-matrix for an N-port network is a square matrix of dimension N, having 2N terminals or equivalently N + 1 using a common reference terminal.

An example of a 4-port S-parameters, representing a generic aggressor-victim pair, is reported in Figure 2.4.

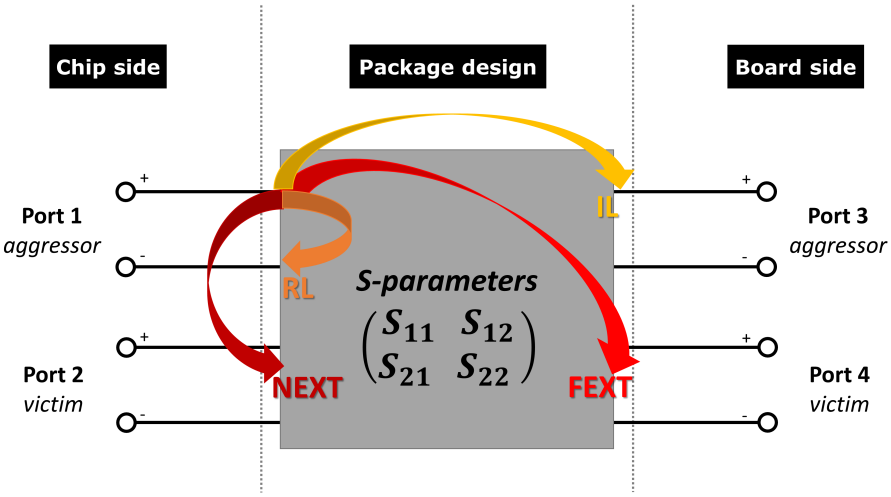

Figure 2.4 S-parameter model for a typical aggressor-victim configuration.

The main elements of the S-matrix are defined as follow:

- S_{11}, S_{22} is a measure of how much of the signal is reflected (ratio between reflected and incident wave), referred to as *return loss (RL)*.
- S_{31}, S_{42} is a measure of how much of the signal is transmitted (ratio between transmitted wave and input wave), referred to as *insertion loss (IL)*.
- S_{21} is a measure of the coupling, referred to as *near-end crosstalk (NEXT)*.
- S_{41} is a measure of the coupling, referred to as *far-end crosstalk (FEXT)*.

The crosstalk depends on which end of the victim line is considered. In particular the backward propagating crosstalk or NEXT is the sum of capacitive and inductive coupling, while forward propagating crosstalk or FEXT is the difference between capacitive and inductive coupling. In general, the S_{21} differs from the S_{41}. This indicates that specifying the crosstalk noise which occurs between two interconnects is not enough, since also the direction matters. The same consideration applies to higher order S-parameter models, which represent more aggressor and victim lines.

However, compared to a distributed modeling approach, in an S-parameters model only local voltage difference is relevant and there is no such a thing like "global ground". Therefore, when used in a SPICE-like circuit simulator, which employs nodal analysis to compute voltages and current referred to a common node (i.e. the 0 level), the reference node of a port is typically set to 0. This means that it is not possible to know the reference voltage and therefore is not possible to handle the power and ground noise separately.

2.3.3 Quality of the S-parameter and integration in a circuit simulator

S-parameters extracted either from measurements or EM analysis may have some quality issues, which affect the stability of the time domain simulation, impacting the reliability of the results. The S-parameter properties that need to be ensured to guarantee a good quality of the model are:

- *Reciprocity*, which means that, according to Lorentz´s theorem of reciprocity, the S-matrix is symmetric for linear circuits with linear isotropic materials:

  $$S_{i,j} = S_{i,j} \text{ or alternatively } S = S^T \quad \text{(for all frequencies)}$$

  Reciprocity metrics of the S-matrix can be computed as mean difference between the elements that have to be equal at each frequency point.

- *Passivity*, which means that the transmitted power, defined as the difference between power transmitted by incident and reflected waves, must be positive for passive networks:

  $$\text{eigenvals } [I - S^*S] \geq 0 \quad \text{eigenvals } [S^*S] \leq 1 \quad \text{(I is the identity matrix)}$$

  Passivity metrics of the S-matrix is computed as the square-root of the maximum of the eigenvals $[S^*S]$.

- *Causality*, which means that the S-matrix does not have to provide a response before the excitation:

  $$S_{i,j}(t) = 0, \; t < T_{i,j}$$

Causality metrics can be derived from the polar plot (i.e. the plot of $\mathrm{Re}\{S_{i,j}\}$ as function of $\mathrm{Im}\{S_{i,j}\}$), observing that a causal system rotates mostly clockwise around local centers.

In addition, it has to be considered that S-parameters, which are basically frequency domain data, are difficult to be directly integrated into a SPICE-like simulator, resulting in longer transient simulation time and potential convergence issues. Macro modeling techniques (such as vector fitting [47]), which typically approximate a multiport S-parameters by rational functions, are commonly used to improve the quality of tabulated S-parameters data, and to fix minor passivity and causality violations thus enabling faster and more stable transient simulation [48], [49].

Chapter 3

AMS SoC-package co-simulation methodology

Reliable and accurate prediction of the system-level behavior through chip-package-board co-simulation methodology is essential to detect potential specification violation issues in the early phase of the development cycle, providing guidelines for both on-chip and off-chip designs in order to achieve "right first time" solutions reducing costs and time-to-market. Sensitive analog/mixed-signal circuits may experience noise coupling at any level of the chip-package-board interconnect path when integrated in a complex SoC design, which includes several fast switching circuits.

In this chapter the focus is on the co-integration of a power converter module and a pure mixed-signal block such as the analog-to-digital converter (ADC). A co-simulation methodology employing a modeling approach at different levels of abstraction is developed to investigate potential crosstalk issues at package-level and to quantify the impact of the DC/DC converter operation on the RMS-noise performance of the ADC analog channels.

3.1 IP blocks description and modeling approach

An automotive SoC design typically requires several high accuracy analog-to-digital converters (ADCs), which are key blocks to sense and process the external inputs in order to quickly react at system-level.

For instance this is essential in ADAS applications due to safety requirements. However, those ADCs need to be integrated in a complex environment that comprises many different fast switching IP blocks (e.g. power converter module), which can act as potential aggressors.

As an application example the DC/DC converter module, which can rapidly switch large charging and discharging currents (di/dt), is considered as aggressor, while the victims are the analog inputs of the ADC module. The system-level ADC performance is characterized in terms of RMS-noise for each analog input channels. This is defined as the standard deviation of the ADC output code compared to the ideal one and is expressed in terms of least significant bit (LSB). A comparison between the typical behavior of the ADC analog inputs when the DC/DC converter is enabled or disabled is reported in Figure 3.1.

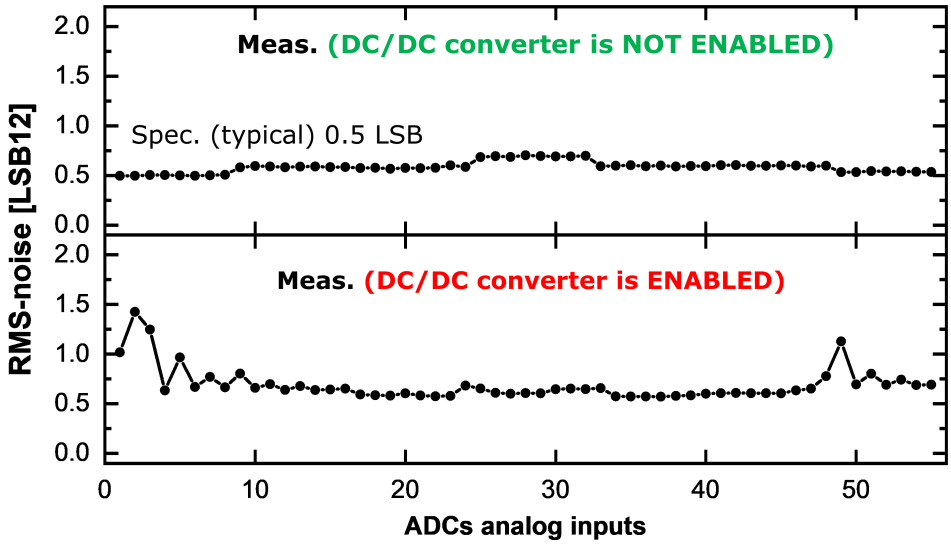

Figure 3.1 Impact of the DC/DC converter on the ADC RMS-noise performance.

It can be seen that some analog inputs experience an increased RMS-noise value (up to 1.5 LSB) compared to the typical stand-alone performance of approximately 0.5 LSB, leading to a specification violation issue at system-level.

3.1.1 DC/DC converter module operation and modeling approach

The DC/DC converter module considered is a DC/DC step down (buck) converter. It is designed to convert the input battery voltage V_{in} (typically from 5 to 7 V) into the core voltage (about 1.2 V) to supply the circuits inside the chip at lower voltage. It is working at relatively high switching frequency of 1.8 MHz. The DC/DC converter simplified model is depicted in Figure 3.2. The current loops of the gate drivers during charging and discharging phase are highlighted by solid and dashed arrows, respectively.

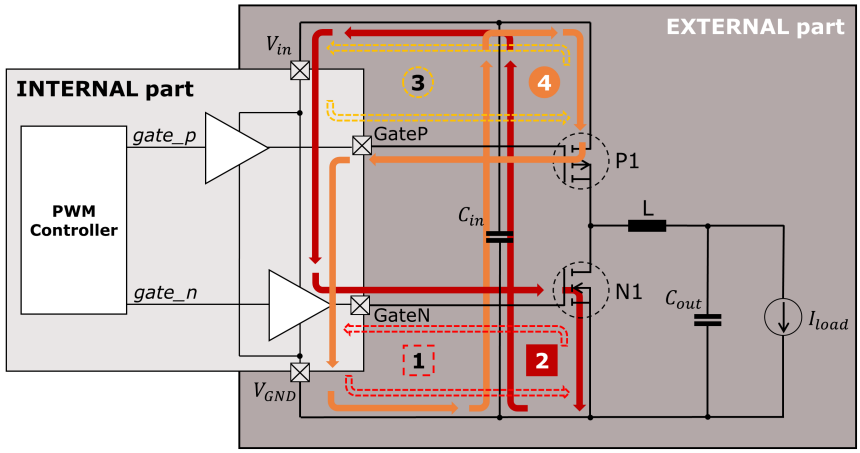

Figure 3.2 Simplified model of the DC/DC buck converter.

The DC/DC module consists of an integrated and an external part. The integrated part includes the pulse-width modulation (PWM) controller block and the drivers for GateP and GateN. The external part includes the filter inductor L, output capacitor C_{out}, the input buffer capacitor C_{in}, and the MOSFET switches. In order to correctly simulate the behavior of the gate driver signals, the MOSFET models contain parasitic inductances at drain and source, gate resistance, gate-source/gate-drain and drain-source capacitances as well as the model of body diode, including its reverse recovery behavior.

The DC/DC converter operation is divided into 2 phases, the charging and the discharging of the external components L and C_{out}. The controller block calculates

the required duty-cycle of the PWM signal which controls the drivers GateP and GateN. The drivers control the switching of the external MOSFETs P1 and N1. During the charging phase, transistor P1 is ON and charges the inductor L from the voltage difference (V_{in}-V_{out}). During the discharging phase, transistor P1 is turned OFF, transistor N1 is ON and the energy from inductor L is discharged into the output capacitor C_{out}. During the switching process, drivers GateP and GateN build the current loops which generate the electromagnetic disturbance due to the fast di/dt and dv/dt transitions. These disturbances can influence susceptible signals which are routed close to the DC/DC converter signals at package-level.

The current loops of the gate drivers are highlighted in Figure 4.2 namely (1), (2) and (3), (4) for GateN and GateP driver, respectively. During the charging phase, GateP driver activates its transistor P1, triggering current to flow in the loop (4) of GateP driver, ground V_{GND}, the buffer capacitor C_{in}, and the gate-source capacitance of P1. When the PWM signal is going low, the GateP driver starts to de-activate the transistor P1 through the loop (3) of gate-source capacitance of P1, power supply V_{in}, and high-side components of the driver. After the transistor P1 has been switched OFF, the transistor N1 is activated by GateN driver. The GateN starts to charge the N1 gate through the loop (2) from high-side of the driver, the gate-source capacitance of N1 and buffer capacitor C_{in}. Before another PWM cycle starts, the GateN driver starts to discharge the N1 gate forming the loop (1) through the low-side of the driver and gate-source capacitance of N1. When N1 is OFF the GateP driver starts to activate the P1, so the cycle repeats itself.

3.1.2 ADC module operation and modeling approach

The ADC module provides a series of analog input channels (from about 50 up to 100 depending on the version of design) connected via an analog input multiplexer to several clusters/blocks of ADC which can operate either independently from each other or synchronized for parallel conversion. The ADCs are based on the successive approximation register (SAR) principle to convert analog input values into discrete digital values, having 12 bit resolution (r) with up to 8/16 analog input channels each and a full-scale input range (FSR) from 0V up to the analog voltage reference (5 V in the case of high voltage range). Therefore, the least significant bit (LSB) is given by:

$$1 \text{ LSB} = \frac{V_{\text{FSR}}}{2^r} \sim 1.2207 \text{ mV}$$

The conversion of an analog input voltage to a digital value can be summarized by two main phases: sample phase and conversion phase. The simplified electrical model used for the ADC module is shown in Figure3.3.

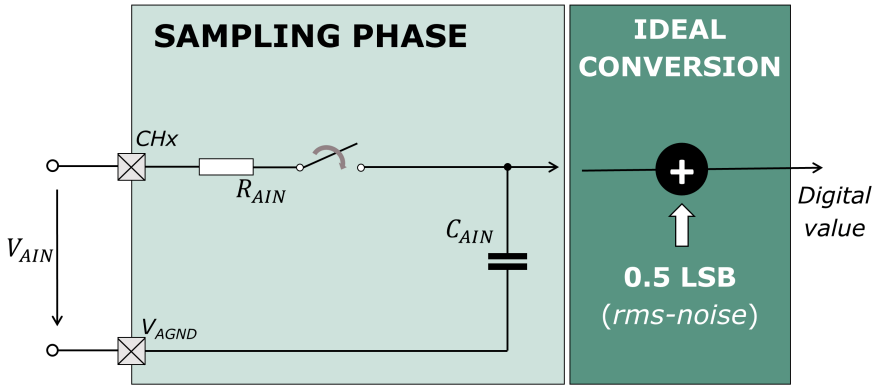

Figure 3.3 Simplified model of the analog-to-digital (ADC) converter.

During the sample phase, the input multiplexer connects the selected analog input to a switched capacitor network, which is used for the sample-and-hold function. Since the main focus is on potential noise coupling at package-level it is sufficient to consider only the impedance seen from the analog input of the ADC, which can be modelled as a low-pass R-C filter. The capacitor C_{AIN} models the switched capacitor network, while the ideal switches with a series resistance R_{AIN} model the input multiplexer. The analog input to be converted is represented by an ideal voltage source V_{AIN}.

During the conversion phase, the stored voltage is converted to a digital value by comparing the analog input voltage with the effective digital approximation of this voltage. However, since we are interested in the analog input voltage held on the sampling capacitor before the subsequent conversion to a digital value, the ADC conversion is assumed “ideal”. In particular, the conversion process is modeled by a block that models the effect of quantization error employing a round-to-nearest method.

Finally, a 0.5 LSB Gaussian random noise is added to the output of the model in order to represent the intrinsic noise-floor of this ADC architecture. The assumption of ideal conversion enables system-level simulation throughout a wide range of samples, which is not feasible with full transistor-level models due to the limits of hardware and software available for simulation-purpose.

3.2 Package-board description and modeling approach

An overview of the physical dimensions and the stack-up information for the investigated package and board designs is reported in Figure 3.4.

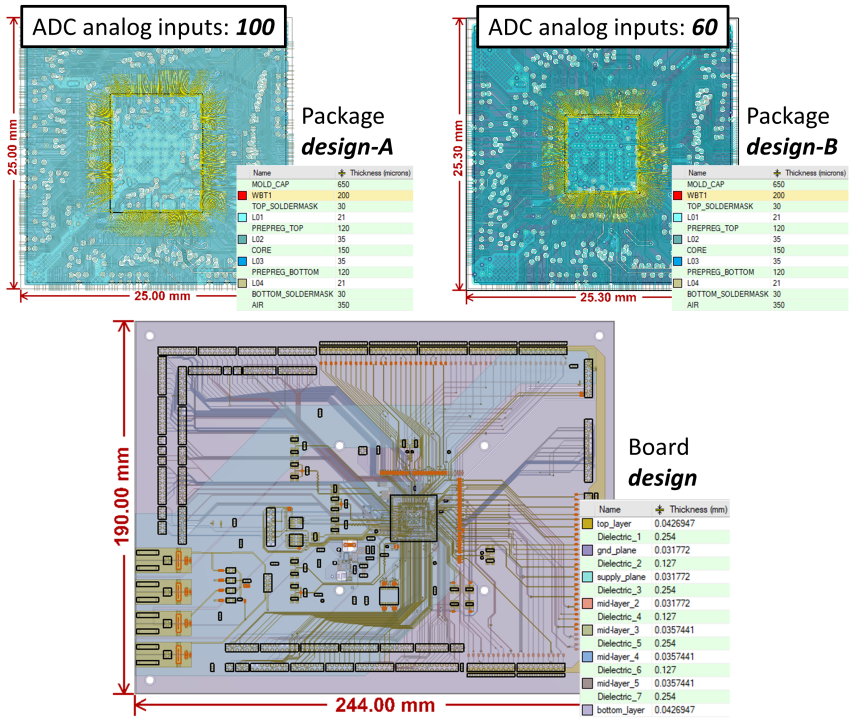

Figure 3.4 Overview of packages and board design along with stack-up information.

In particular, two package design derivatives are considered: design-A having about 100 ADC analog input channels and design-B having about 60 channels.

The package technology in our example system is a wire-bond ball grid array (BGA). The package design features 516 pins and it consists of a 4 metal layer laminate substrate having power and ground planes on the inner layers, while the signals are routed on the top and the bottom layer. The board, commonly referred to as printed circuit board (PCB), consists of an 8 layer laminate design having a complete ground plane on the second layer and the different power planes for the different voltage domains on the third layer.

3.2.1 Modeling approach

The modeling approach via EM field solver is essentially determined by the switching behavior of the gate driver signals of the DC/DC converter and the physical dimensions of the package-board interconnect design. The ANSYS EM Suite is used for package and board parasitic extraction [50].

As described in chapter II, most of the energy of a signal is contained inside the spectrum from DC to the knee frequency. Considering the DC/DC converter gate driver signals rise time (in the order of 1 ns), the highest relevant frequency is estimated as:

$$f_{\text{knee}} \approx \frac{0.5}{t_{\text{rise}}} \approx 500 \text{ MHz}$$

Furthermore, considering that some internal nodes may switch at higher frequency (about 100 ps) a maximum frequency of 5 GHz is extracted via EM field solver to ensure proper transient simulation. Therefore, the corresponding wavelength is about $\lambda \cong 30$ mm. Since the physical dimensions of the package and board nets are comparable to the wavelength, a full-wave solution is required.

Two different types of parasitic extraction setup are investigated which consider the package and board layouts merged together in order to preserve the electromagnetic coupling and to consider the impact of the board ground and power planes as current return path.

The *setup-1* involves a hybrid solver (SIwave) to handle the full package-board system complexity. The circuit ports are defined both on chip and board side as summarized in Figure 3.5.

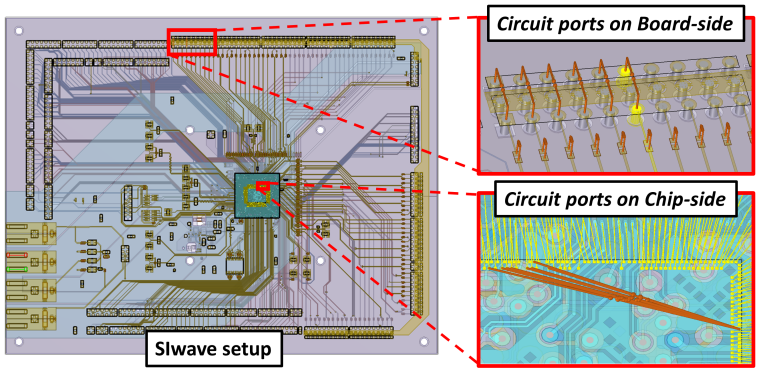

Figure 3.5 Overview of the port definition in SIwave (*setup*-1).

However, such an extraction approach is not considering all the 3D effects that may take place at package level, especially coupling on the power delivery network due to the non-ideality introduced at package level via net routing and wire-bond, compared to an ideal plane structure, as it is implemented on the board.

The *setup-2* involves a more accurate 3D solver (HFSS 3D layout) which allows to handle all the 3D effects taking place at package-level. However, due to the size and complexity of the full-board, in this case, a cut-out of the board under the package is considered (including only the power and ground layers) in order to have a good trade-off between accuracy and simulation time. An overview of the ports setup in shown in Figure 3.6.

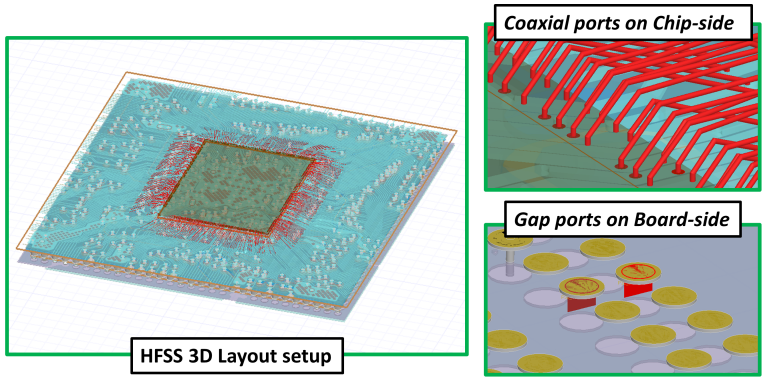

Figure 3.6 Overview of the port definition in HFSS 3D layout (*setup-2*).

Therefore, the package and the board design (considered as whole or cut-out depending on the setup involved) are characterized via S-parameter models, extracted over a wide range in frequency from DC up to the maximum frequency. In particular, a discrete sweep is applied from 1 MHz to 5 GHz, while the DC point is extracted via quasi-static solver (Q3D) for a more precise estimation.

3.3 System-level co-simulation approach

The extracted S-parameters models are then combined together with the simplified DC/DC converter and ADC models described in the previous sections in ANSYS electronic desktop and simulated via a circuit simulator (Nexxim). Therefore, the impact of DC/DC converter switching on the RMS-noise performance of the ADC analog inputs is evaluated by means of a simulation framework, based on a modeling approach at different levels of abstraction as summarized in Figure 3.7.

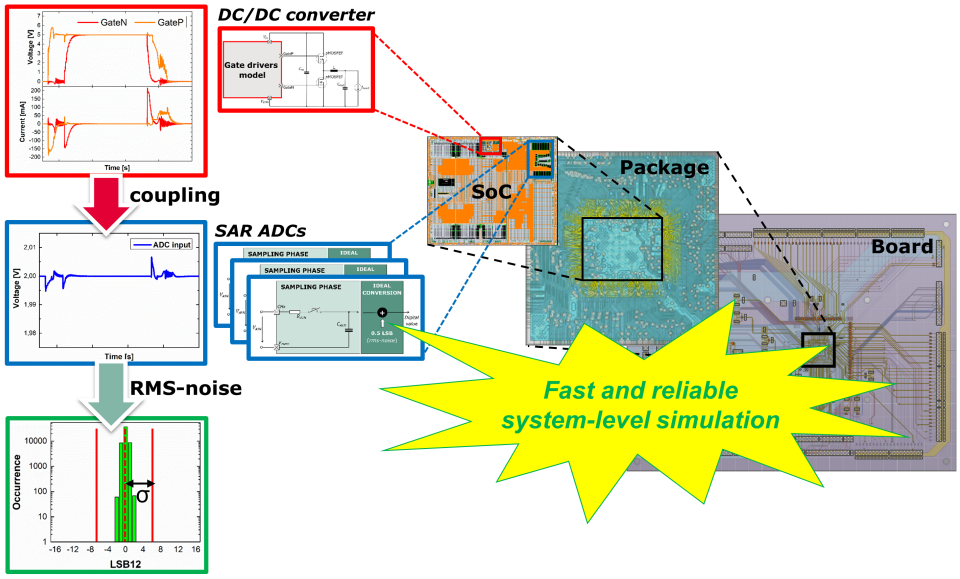

Figure 3.7 Overview of the system-level simulation approach.

A simulation approach at different levels of abstraction is exploited to deal with the complexity of the system-level simulation. Furthermore, a co-simulation methodology is developed to align measurements and simulations.

3.3.1 Co-simulation methodology

Measurements of the ADC RMS-noise performance are carried out using the linear ramp histogram method [51]. An overview of the different measurement steps is summarized in Figure 3.8.

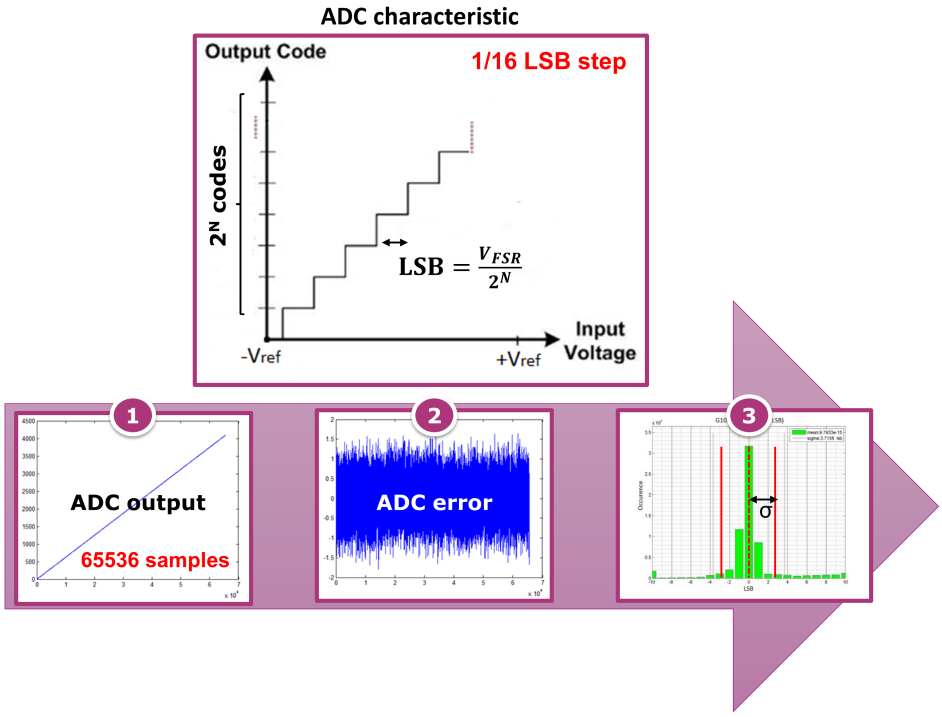

Figure 3.8 ADC characteristic and measurement setup steps.

In particular, the input signal for the measurements is a DC voltage ramp (with 1/16 LSB step) which spans from the negative to the positive reference voltage of the ADC, in order to get a sufficient number of samples for each code transition (i.e. 16 $\times$ 2^{12} = 65536 samples). As a first step, the ADC's output code corresponding to the input voltage ramp are recorded. Subsequently, the error between the measured and the expected output code is computed and expressed in LSB. Finally, the RMS-noise value is computed as the standard deviation of the histogram derived from the ADC´s error distribution [52].

The simulation principle relies on the assumption of uncorrelated aggressor-victim signals, which means that the ADCs can sample each point in time over one switching period of the DC/DC gate drivers (i.e. 550 ns) with the same probability. Therefore, 55000 samples have been collected over one period of the aggressor signals (i.e. 10ps step) while the input of the ADC is fed with a constant DC-value. This allows to build a histogram comparable to the one obtained by measurements, achieving similar statistical information.

This methodology has been validated against post-silicon measurements for different package derivative designs.

3.3.2 Measurements vs Simulations results

Inspecting the measured histogram and the simulated one, it can be seen that the noise is not Gaussian, since in both cases the RMS-noise coverage interval (1-sigma) contains almost 90% of the ADC output code distribution, whereas it would be 68% for a Gaussian distribution. As shown in Figure 3.9, the detailed simulation based on our methodology described above shows excellent correlation with measurement data.

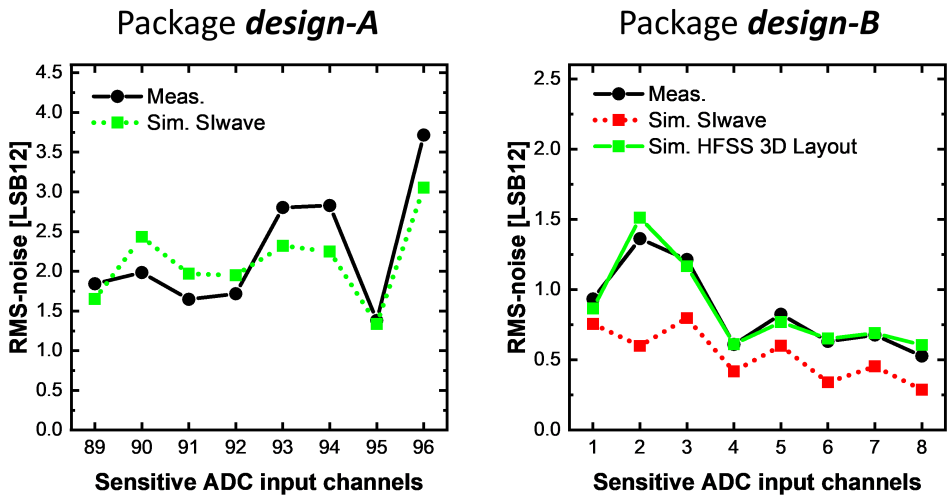

Figure 3.9 Simulation vs. measurements comparison for the most affected ADC inputs.

In particular, it is found out that the package and board characterization via the *setup-1* (i.e. employing a hybrid solver) allows to achieve good correlation with measurements data for the most affected channels of the package design-A, whereas it fails to properly model ADC channels for a sub-set of sensitive channels of package design-B. For the latter case, the *setup-2* (i.e. using a 3D full-wave solver) is required to achieve a good match with measurements data.

A comparison for the whole ADC analog inputs of the package design-B is provided in Figure 3.10.

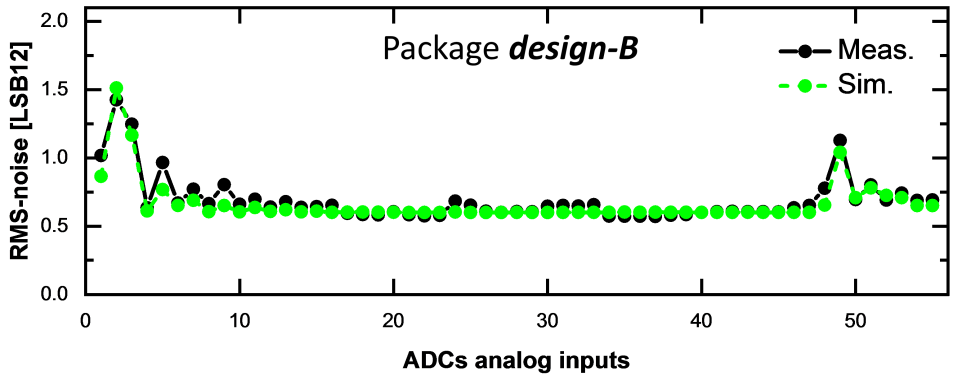

Figure 3.10 Simulation vs. measurements comparison for the whole ADC analog inputs.

The detailed simulation, based on our methodology described above, employing the *setup-2* for package-board parasitic extraction, shows an excellent correlation with measurement data for all the ADC analog inputs.

3.4 Conclusions

This analysis assessed the potential of the Chip/Package/Board co-simulation methodology to predict ADCs performance in terms of RMS-noise when the DC/DC converter is enabled. An accurate simulation approach based on a simplified model for the circuit modules along with the S-parameter for the package-board layout is proposed, and two different parasitic extraction setups are validated against measurements data. The discrepancy between the two simulation setups when compared with measurements from the package design-B can be ascribed to the different coupling

mechanism underlying the RMS-noise behavior for the ADC analog channels sub-set. When the ADC channels are mainly affected by signal-to-signal coupling, a hybrid solver can provide adequate accuracy, but when those channels are mainly affected by power-to-signal coupling the full-3D solver is required. A more comprehensive discussion about the different coupling mechanism and how to detect and mitigate them is provided in the next chapter.

Chapter 4

A step-by-step chip-package co-design methodology

Going beyond the traditional approach used in package design, based on layout guidelines, in this chapter a chip-package co-design methodology is developed to optimize the final design. Optimization is achieved thanks to the identification of the main coupling mechanisms and pointing out their exact location at package-level. A step-by-step approach is developed to identify first the most affected ADC analog inputs and subsequently the main coupling mechanism by inspecting the distribution of the ADC noise for the most affected analog channels. Then, the loop mutual inductance is extracted for the different segments of the package nets, revealing the critical regions that need to be optimized to effectively mitigate the impact of the DC/DC converter gate drivers current, returning through the corresponding power/ground nets. Measurements, carried out on a laminate ball grid array (BGA), have proven the effectiveness of such a methodology to identify and optimize the most severe coupling paths (mainly due to inductive coupling) between the gate drivers of the DC-DC converter and the ADC analog inputs.

4.1 Identification of the most severe coupling path

Identifying the most severe coupling path as shown in Figure 4.1, before applying the co-simulation methodology described in the previous chapter, allows to avoid the

S-parameters extraction for the whole ADC analog inputs in a given package design. This in turn enables an efficient assessment during package development.

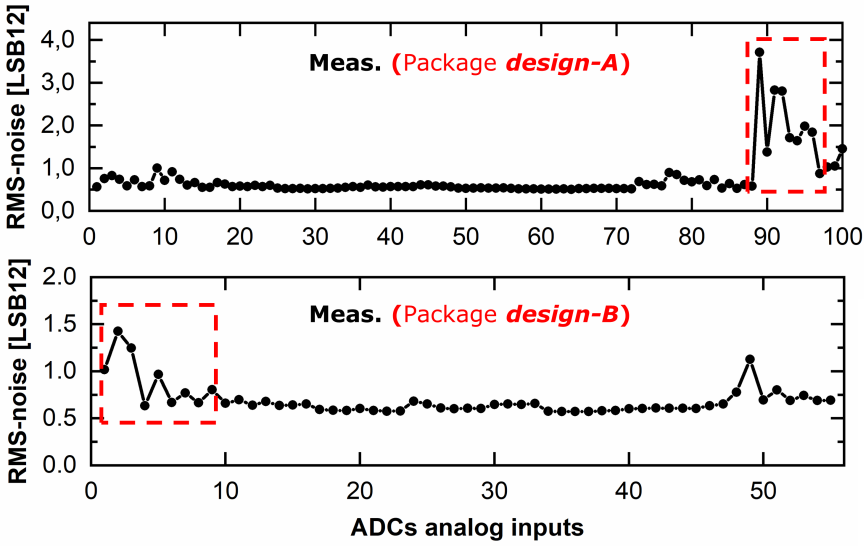

Figure 4.1 Measured ADC analog inputs RMS-noise behavior.

Looking at the noise signature for the most affected ADC analog inputs it can be noted that the noise profile follows the switching current behavior of the DC/DC converter's gate drivers and power supply (see Figure 4.2).

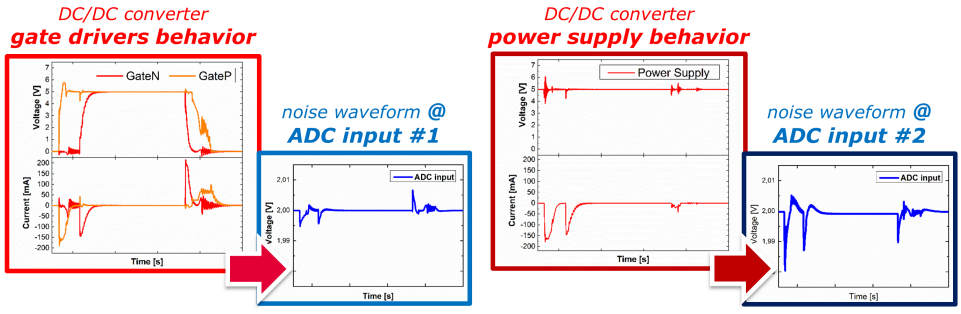

Figure 4.2 Noise behaviour at the ADC inputs when the DC/DC converter is switching.

Therefore it can be concluded that the coupled noise is mainly due to inductive coupling. The extracted loop mutual inductance at 100 MHz is reported in Figure 4.3 from which the most affected ADC analog inputs can be identified.

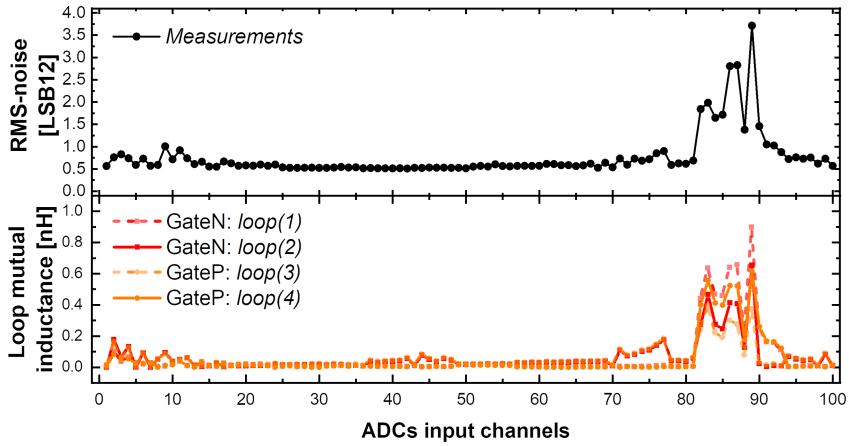

Figure 4.3 Comparison of the extracted mutual loop inductance and RMS-noise.

In addition, from Figure 4.4, it can be seen that the highest RMS-noise value measured correlates with the maximum peak of loop mutual inductance.

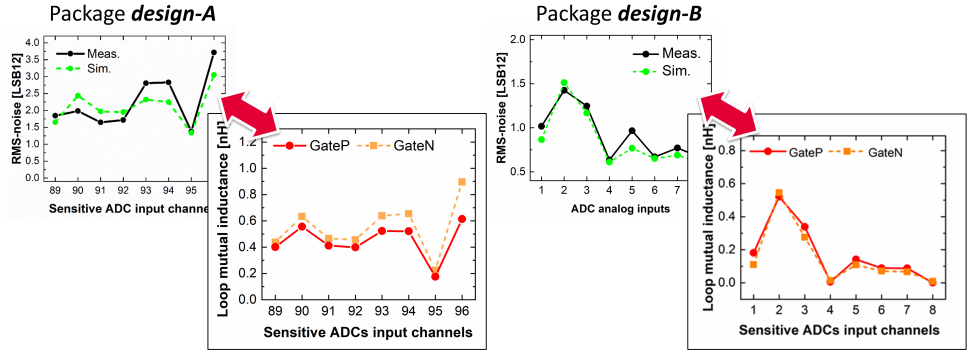

Figure 4.4 Extracted mutual loop inductance for the most affected ADC analog inputs.

Measurements of the RMS-noise at the ADC analog inputs when the DC/DC converter is enabled, show a direct correlation with the extracted loop mutual inductance between the DC/DC converter gate drivers and the ADCs analog inputs. Therefore, the loop mutual inductance between the outputs of the DC/DC converter gate drivers

and the inputs of all the ADCs, can be used as a first order estimation of the most severe coupling paths in package designs.

In particular, the noise behavior at the ADC analog input is expected to be shaped by the DC/DC converter frequency disturbances up to the cut-off frequency of the sample-and-hold filter, which is typically below 100 MHz for the SAR ADC implementation considered here. Therefore, a quasi-static solver (Q3D) has been used to extract the inductance matrix (self and mutual terms), considering the corresponding return paths for aggressor and victim signals. However, Q3D only extracts the partial inductance matrix; therefore, proper matrix reduction is applied to estimate the loop mutual inductances [53], [54] of the identified current loops.

4.2 Detection of the coupling mechanisms

Since real current always flows in a closed loop, both the signal path and the return path must be considered. Figure 4.5 reports the simulated loop mutual inductance (@ 100 MHz) between the DC/DC converter gate drivers and the most sensitive ADC analog inputs, highlighting the impact of the real return current path (assumed to be in the closest power/ground net at package-level).

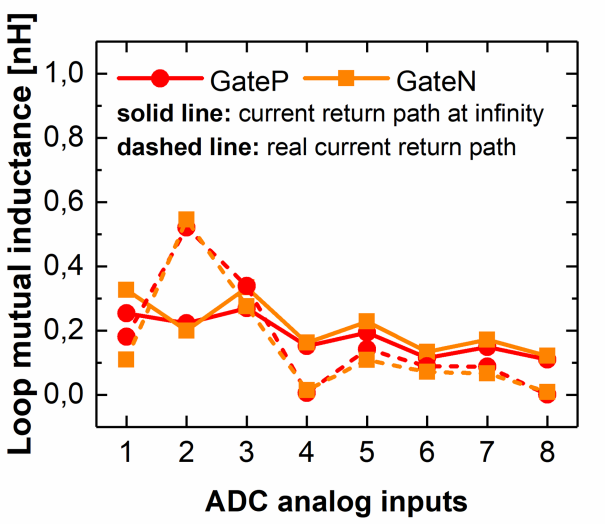

Figure 4.5 Loop mutual inductance comparison for ideal and real return path.

In particular, two cases are highlighted: when only the DC/DC gate drivers signal path is considered (solid line) (i.e. the return current loop is assumed to be at infinity) and when the real return path through the closest power/ground nets of the package is considered (dashed line). It can be seen, from the inductive coupling on the second ADC analog input, that the DC/DC gate drivers current returning through the closest power/ground nets contributes to additional coupling. Therefore, the mutual inductance can be used to identify the main coupling mechanisms: if it is dominated by signal coupling or by coupling from the power supply nets.

The impact of the return path through the power/ground routing at package-level is also reflected in the ADC histogram. Applying the co-simulation methodology described in chapter III, the histogram for the most affected analog input is shown in Figure 4.6.

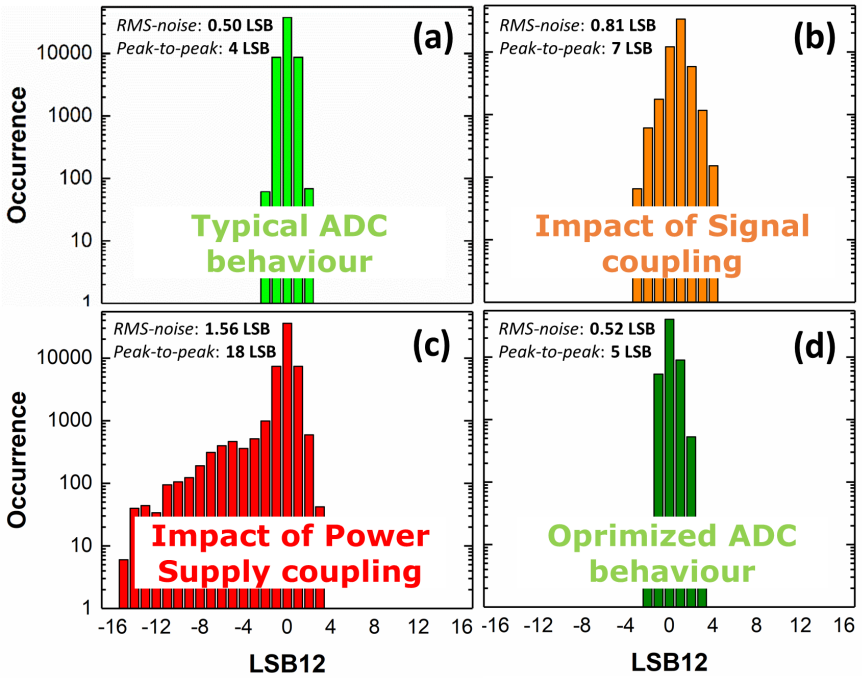

Figure 4.6 Impact of the noise coupling on the ADC analog input histogram.

In particular, the noise distribution of the ADC in absence of noise coupling (assumed to be a Gaussian with RMS noise of 0.5 LSB) (a) is compared to the

histogram obtained when only the current of the DC/DC gate drivers signal is considered without the real return current path (b) and when the return path is assumed to be in the closest power/ground package nets (c). Figure 4.6 (d) shows the impact of an optimally designed power/ground return path (as reported later in this chapter) that allows to obtain a noise histogram closer to the one of the isolated ADC.

In summary, it can be concluded that an ADC histogram with heavier tails, approximately symmetric around its mean value, is an indication of noise coupling mainly from a switching signal with no significant mitigation/influence from the power/ground return path design. Instead, an ADC histogram with heavier tails skewed to the left, is an indication of a significant noise coupling from the return path due to the current drawn (i.e. always in the same direction) from the power/ground nets. Therefore, a careful design of the power/ground nets is required in order to effectively provide shielding of the DC/DC gate drivers net and not to contribute additionally to the total amount of coupled noise.

4.3 Package elements optimization

In order to identify the package design parts that need to be optimized, the loop mutual inductance between the DC/DC converter gate drivers and the most sensitive ADC analog input is extracted. In particular, each signal and its return path through the corresponding power/ground nets, is considered for the different segments of the package nets in the original design. An overview for the most affected channel is reported in the table below.

M_{loop} [nH]	*bondwires*	1^{st} *layer*	*via*	4^{th} *layer*
	GateP/GateN	GateP/GateN	GateP/GateN	GateP/GateN
Original design	**-0.15 / -0.13**	**-0.4 / -0.4**	< 0.01	< 0.05
Re-design	**-0.15 / -0.13**	-0.08 / -0.07	< 0.01	< 0.05
Optimized design	0.06 / 0.05	-0.05 / -0.04	< 0.01	< 0.05

Table 4.1 Loop mutual inductances between the DC/DC converter GateP/GateN and the most affected ADC analog input for different package designs.

Each package signal net consists of a bond wire, followed by a first layer routing (above the corresponding ground plane) connected through a via to the fourth layer routing (below the corresponding power plane) which is connected to the ball. A 3D view of the package layout with focus on the aggressor-victim nets is reported in Figure 4.7 (a).

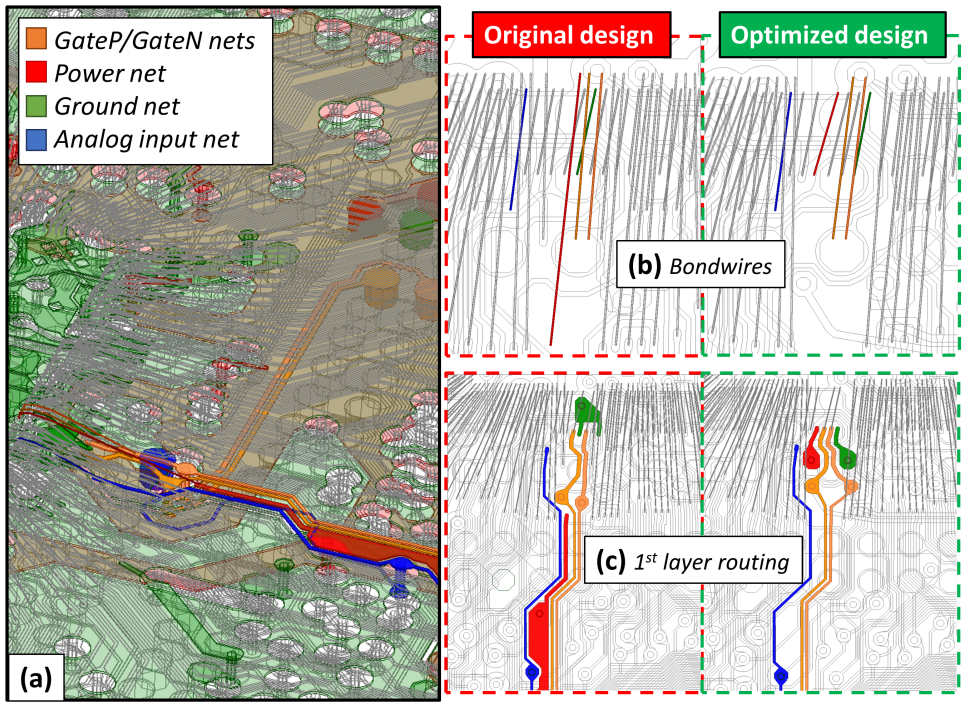

Figure 4.7 Overview of the package design-B and main modification applied.

It can be seen, that most of the inductive coupling takes place on the bond wires and on the first layer routing (up to the via). Negative values in the table indicate that the coupling from the aggressor return path through power/ground nets dominates the one which stems from the aggressor signal net within the investigated current loop. Please note, that the loop mutual inductance is computed considering both contributions from the aggressor signal and its return path to the signal and the return path of the victim net, as follows:

$$M_{\text{loop}} = M_{A-V} - M_{\text{RA}-V} + M_{\text{RA}-\text{RV}} - M_{A-\text{RV}}$$

Where M_{A-V} and $M_{\mathrm{RA}-V}$ are the partial mutual inductances contributed from the aggressor signal and its return path to the victim signal, respectively, while $M_{A-\mathrm{RV}}$ and $M_{\mathrm{RA}-\mathrm{RV}}$ are the partial mutual inductances contributed from the aggressor signal and its return path to the victim return path. Therefore, it can be concluded that proper choices of pad locations, bond wires profile, and first layer routing are essential to minimize the impact of the DC/DC converter on sensitive lines routed nearby. Specifically, an optimal design of the package (i.e. minimizing the loop mutual inductance) can significantly reduce the impact on the sensitive signal routed close to the DC/DC converter, without significantly affecting the ADC performance.

4.3.1 Proof of concept for re-designed packages

The expected improvement from a re-design of the package design-A is reported in Figure 4.8 (improved routing of the aggressor/victim nets for reduced inductive coupling path) together with correlations of RMS-noise measurements data.

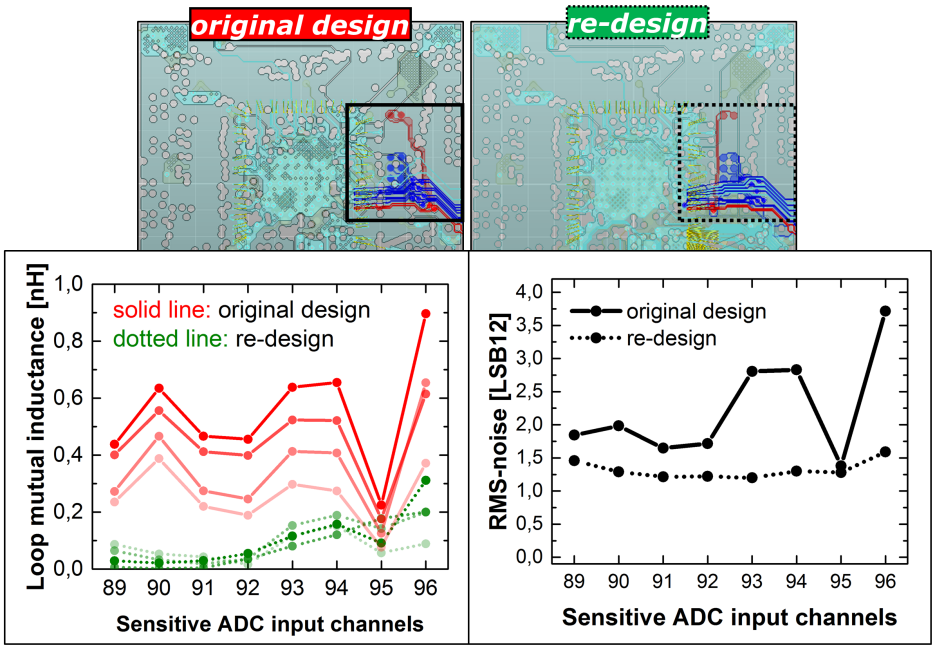

Figure 4.8 Improved design for package design-A.

It can be seen that the extracted mutual loop inductance correlates very well with the improvement achieved and verified by measurements.

A re-design of the package has been implemented, acting on the first layer routing, since the bond wire profile and pad positions could not be changed at this design stage. Consequently, only the mutual coupling on the first layer (which was the major contributor to the total inductive coupling on the most affected victim, as reported in table I) has been re-designed, resulting in a significant noise reduction (see Figure 4.9). It can also be seen that the predicted improvements are in good agreement with measurements.

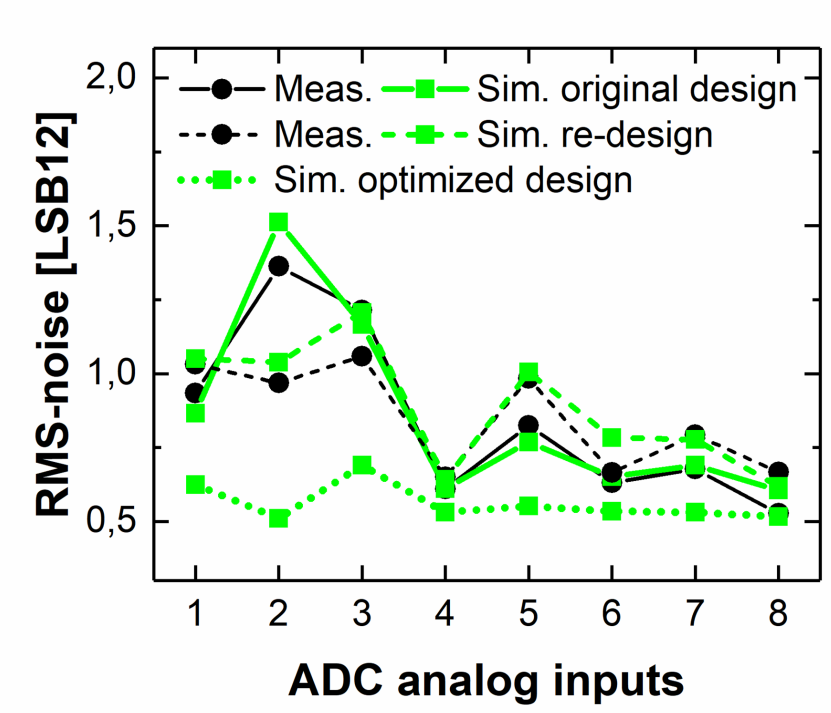

Figure 4.9 Comparison of measurements and simulations for package design-B.

Finally, as reported in Figure 4.7 (b) and (c), a further optimization of the design has been performed in order to demonstrate the potential of the developed methodology for future package design in order to mitigate crosstalk issue in the early stage of the design process. Specifically, two similar bond wire profiles are

considered for power and ground, which are located on the sides of the gate drivers, while using the first layer routing to balance the difference in mutual contributions that arise from the bond wires. The expected improvements are also reported in Figure 4.9, showing that the DC/DC converter now has almost no impact on the ADC RMS-noise performance of the analog inputs routed nearby the gate driver signals at package-level.

4.4 Conclusions

Differently from the traditional approach, where general rules of thumb are provided like “avoiding big current loops” or “keeping aggressor and victim nets as far apart from each other as possible”, a step-by-step simulation methodology is proposed to guide the package design. The main noise coupling mechanisms (from a signal or a power/ground net) can be identified from the distribution of the ADC noise, while the package layout locations which need to be optimized, can be identified by extracting the mutual loop inductance for each segment of the package nets. In this way, the DC/DC converter impact on the most sensitive ADC analog inputs has been successfully mitigated.

Exploiting such a methodology during the package design development might lead to longer design cycles due to an increased number of engineering-change-order (ECO) loops. However, the final optimized chip-package design enables smaller package size, ensuring power and signal integrity with minimum number of routing layers, which in turn saves cost of the final product. Furthermore, considering that the customer fixes the package ball-out for backward compatibility reasons, potential specification violations can be predicted earlier in the product development cycle while designing chip and package in parallel. This allows to quickly react if changes at concept-level are needed (e.g. synchronization between IP blocks) or if adjustment of the system level specifications are agreed with the customer, reducing the cost of the design development and consequently time-to-market too.

Chapter 5

Machine learning approach for chip-package co-design

Nowadays automotive SoCs are designed to enable data acquisition from surrounding sensors (sensors fusion) and process them in real-time to take the proper counter-measures at system-level. Many applications such as object recognition and edge detection, which are required to support autonomous driving, are based on machine learning algorithms to deal with the complexity of the task and to take faster decision.

Machine learning approaches started also to be introduced during the development of a SoC design in order to deal with complexity and simulation time. An overview of the applications to common electronic circuits is provided in this chapter. Amongst many machine learning algorithms, which belong to the class of supervised learning, the support vector machine is considered for potential application in a chip-package co-design methodology due to its robustness against high variability in small training-sets.

5.1 Machine learning approach and applications to chip-package development

Machine Learning (ML) algorithms can be categorized in several types [55]. In particular, four main categories can be identified:

- *Supervised learning*, which tries to map a given set of variables (commonly referred to as features) to a given target variable (referred as label).
- *Unsupervised learning*, which tries to cluster the data since the target variable to be predicted is not available.
- *Semi-Supervised learning*, which tries to combine both the supervised and unsupervised learning algorithm to address both labeled and not labeled data.
- *Reinforcement learning*, which tries to self-train the model using a trial and error strategy to learn from past experience.

Here the main focus is on supervised learning algorithm. An overview of the learning process is reported in Figure 5.1

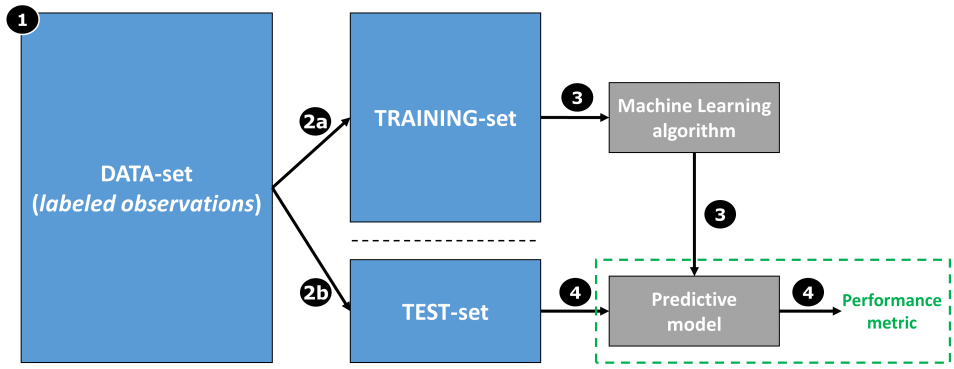

Figure 5.1 Sketch of the supervised machine learning process.

In a supervised learning problem, a data-set consisting of labeled observations is available *(1)*. Subsequently the data is separated in a training data-set *(2a)* on which the model is trained *(3)* and a test or validation data-set *(2b)* against which the model is tested *(4)*. In particular, depending on the prediction problem (i.e. target variable) we can distinguish between a classification problem (i.e. the model has to predict a discrete target variable, often called classes) and a regression problem (i.e. the model has to predict a continuous target variable).

Therefore, based on the available data and the problem formulation, different algorithms can be used, such as Support Vector Machine (SVM), Regression, Decision Tree or Artificial Neural Network (ANN) amongst many others.

5.1.1 Applications overview: from transistor-level to system-level behavior prediction

Machine learning algorithms can be used to provide fast prediction of the behavior of an electronic circuit for design space exploration and optimization, avoiding a series of complex and time consuming circuit simulation. Amongst several machine learning algorithms many research works demonstrated the artificial neural networks (ANNs) to be a valid approach for device and circuit level modeling [56], which have been widely applied to macro modeling of non-linear microwave circuits [57], [58].

The application of ANNs ranges from active device characterization [59] such as modeling of GAN power transistors [60] to behavioral modeling of analog circuits such as basic current mirror structures and a differential amplifier [61] or more complex CMOS band-gap voltage reference [62], including sizing strategies [63], as well as non-linear mapping between design parameters and performance of high-speed interconnect systems, in order to overcome the traditional time-consuming Monte Carlo simulations and speed up the design optimization [64]. Recent works [65], [66] have demonstrated the validity of a correlation-based feature selection algorithm combined with a multilayer perceptron ANN to predict eye height (EH) and width (EW) of high-speed SerDes (HSS) channels (SATA 3.0 and PCIe Gen3) based on S-parameters data. In [67] the support vector machine (SVM) algorithm has been investigated for the modeling of high-speed interconnects with largely varying and/or highly uncertain design parameters. As a main outcome the SVM regression model resulted to be a valid solution when a small number of training samples is available.

5.2 Main challenges towards a good data-set

The data-set is one of the most important parts in machine learning since the performance of the predictive model results to be as good or as bad as the quality of the data used for the training of the model, independently of the chosen algorithm.

Therefore, data quality is essential to build an effective machine learning model, and data visualization (e.g. see if a feature is correlated to the output or correlated with the other features) may help to identify the best strategy to optimize the prediction performance. However, data-sets may present problems such as:

- *Imbalanced data*
  One crucial problem in many real applications for machine learning is the presence of class imbalance in the data-set (i.e. the samples are not equally distributed among the different classes) [68]. The main implication is the poor performance of chosen classifier, which tend to ignore the minority class samples, because most classifiers assume an equal distribution of the samples amongst classes and therefore an equal misclassification cost.

- *High dimensionality and correlation*
  High dimensional data-set (i.e. higher number of features compared to the total number of samples) may lead to an increased training time and poor prediction performance. Furthermore, when dealing with high dimensional data-sets, removing non-correlated features and using fewer features, but highly correlated with the output, may significantly improve the prediction performance, while reducing the training time. However, high correlation between features may lead to instability of the model, since small changes in the training set result in dramatic changes in the selected subset of features.

Therefore, the data-set size and characteristic as well as the problem formulation (classification or regression problems) drive the choice of the machine learning algorithm which ensures the desired prediction performance.

5.2.1 Common methods to address imbalanced data-set

Different methods have been developed to address such a problem, targeting to improve either the data-set or the algorithm. An overview of those methods can be found in [69]. The methods targeting the *improvement of the data-set* try to balance the distribution of the classes in the data-set either by over-sampling the minority class and/or under-sampling the majority class. The research results presented in [70], [71]

report that under-sampling the majority class leads to a better classifier performance rather than over-sampling the minority class. However, this approach may lead to the loss of relevant trend from the original data-set or model over-fitting. A combination of the two is proposed in [72], where a synthetic minority over-sampling techniques (SMOTE) is developed and combined with the common method of under-sampling the majority class, achieving better classifier performance than only under-sampling the majority class.

Instead, the methods targeting the *improvement of the machine learning algorithm* try to learn more information from the samples which belong to the minority class by using a cost-sensitive classifier which assigns a high cost to the misclassification of a sample from the minority class. The main benefit of this approach is that it doesn´t affect the original data distribution. However, the main challenges are the precise determination of the misclassification cost (which is also affected by the feature set and the intrinsic parameters of the classifier model) [73] and the gap between the performance assessment metric and the objective of the training on the imbalanced data-set [74].

As a potential solution to overcome these challenges, [75] proposes an effective wrapper framework for training a cost sensitive SVM classifier driven by the imbalanced evaluation criteria (applied to the objective function) to improve the classification performance by simultaneously optimizing the best feature subset, intrinsic parameters, and misclassification cost parameters. Therefore, it is worth to notice the importance of feature selection for problems of class imbalance. In particular, wrapper and embedded methods have been found to be a good approach in handling the class imbalance problem [76].

5.2.2 Feature selection to address dimensionality reduction and correlation

Feature selection is used to reduce the dimensionality of a data-set by selecting a relevant sub-set of features, subject to constraints on the required or excluded features. Feature selection methods can be categorized into:

- *Filter methods*, which use only the intrinsic characteristics of the features measured via univariate statistic (e.g. feature variance and feature relevance

to the response). This method is typically used as a data pre-processing step, therefore this type of feature selection is uncorrelated to the training algorithm.

- *Wrapper methods*, which select a subset of features and then add or remove features using a selection criterion based on the classifier performance.
- *Embedded methods*, which similarly to the wrapper method optimize the objective function or the performance of the learning algorithm, but learn feature importance as part of the model learning process. Therefore, this type of algorithms selects features that work well with a particular learning process.

Many research works exploited the joint development of SVM model and feature selection [77], [78], [79], [80] resulting in a significant reduction of features while keeping good classification performance, because the features that are not directly contributing to the performance are removed. A performance comparison of combining various feature selection strategies (either simple or wrapper-methods) with SVM is reported in [81]. In particular, one of the most popular feature selection algorithms in order to deal with high dimensional data-set is the sequential feature selection method, reported in Figure 5.2

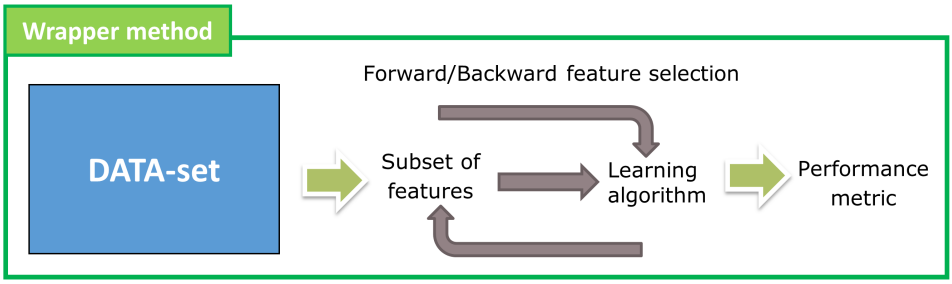

Figure 5.2 Overview of the sequential feature selection algorithm.

In practice, the search algorithm attempts to find an optimal sub-set of features by iteratively selecting or removing features (i.e. forward or backward algorithm, respectively) based on the chosen classifier performance metric. Therefore, this method results to be computationally more expensive than a simple filter approach due to the repeated learning step and cross-validation until the algorithm stopping criteria is satisfied.

However, high correlation amongst features may affect the model prediction performance and its stability [82]. A fast correlation-based filter (FCBF) method is proposed in [83] as a pre-processing step to machine learning algorithm in order to deal with high dimensional data for classification problem. In [84] a correlation bias reduction (CBR) strategy is proposed to improve the performance of the support vector machine recursive feature elimination (SVM-RFE) algorithm. Another approach for correcting the correlation bias is the use of methods for group selection algorithm which combines feature clustering with any classification method [85], [86], [87].

5.3 Supervised learning models: Support Vector Machine

Support vector machines (SVMs), also known as support vector networks, fall into the category of supervised learning methods and are used for classification and regression. The SVM for binary classification problem was presented by Cortes and Vapnik in 1995 [88]. In addition, SVM for the regression problem, referred to as Support Vector Regression (SVR), was proposed in 1996 by Vapnik *et al.* [89]. In particular, the kernel trick was introduced in [90] to create a non-linear classifier in order to deal with data-sets that are not linearly separable. The kernel function allows to map the input data into a high-dimensional space where the data can be linearly separated (common kernel functions are polynomial and Gaussian or Radial Basis Function). Furthermore, in [91], [92] a method to extend the binary classification problem to multi-class classification is proposed by breaking down the problem into multiple binary problems. In practice, a different classification strategy is applied depending on the binary classifier approach (i.e. the binary classifier distinguishes between one class and the other or between every pair of classes). Instead, in [93], [94] a method is proposed to solve a single optimization problem for multi-class classification.

An overview on SVM can be found in [95], while a library for SVM called "LIBSVM" developed since the year 2000 and targeting several issues such as optimization problems, theoretical convergence, multi-class classification and parameter selection can be found in [96]. The main advantages can be summarized as follows:

- *Good generalization performance*, thanks to its regularization capabilities which prevent the model to over-fit the data.

- *Robustness of the model*, because it maximizes the margin, therefore a small change to the data does not greatly affect the performance.
- *Handles non-linear problems*, thanks to the Kernel trick which allows to efficiently classify non-linear data.
- Solves both Classification and Regression problems, employing SVM and SVR, respectively.
- *Works effectively for large number of features*, even larger than the number of samples.

Instead, the main disadvantages can be summarized as follows:

– *Choice of the Kernel function*, can be difficult and complex since it would lead to an increase of error percentage as well as a reduction in the training speed.

– *Training time and memory requirement for large data-sets*, can be long due to the complexity of the algorithm which uses quadratic programming.

5.3.1 Linear Support Vector Machine (SVM) for binary classification

The basic concept behind an SVM model is that the data-set, represented as points in an n-dimensional space is mapped in a way that can be separated into classes using a hyperplane, which acts as a linear classifier. The extreme data points from each class, which are situated on the boundary of the selected hyperplane, are called Support Vectors. Amongst all the potential hyperplanes that may be selected to classify the data, the SVM algorithm is looking for the optimal hyperplane which maximizes the margin between the classes (i.e. the distance of the hyperplane from the nearest data point belonging to any class is maximized). In general, the higher the margin the better the generalization performance of the classifier. Finally, new data points are mapped into that same space and predicted to belong to a class, based on which side of the separating hyperplane they fall.

An overview of the SVM concept is reported in Figure 5.3 for a binary classification problem in a 2-dimensional space.

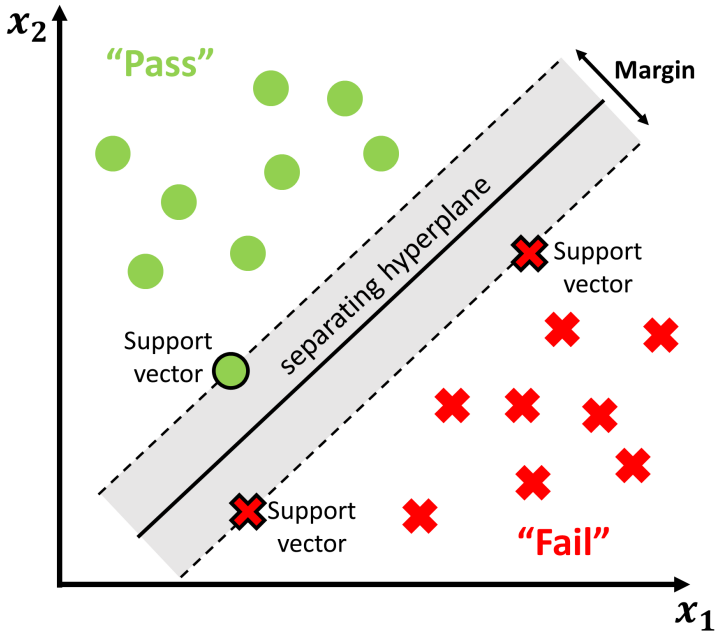

Figure 5.3 Support Vector Machine (SVM) concept.

Given a data-set consisting of m samples of the form $(\bar{x}_i, \bar{y}_i)$ for $i = 1, 2, \ldots m$, where the point $\bar{y}_i$ indicate the binary class (e.g. "Pass" or "Fail") to which the point $\bar{x}_i$ belongs, while $\bar{x}_i$ is a 2-dimensional (x_1, x_2) real vector. The SVM algorithm is looking for an optimal hyperplane which separates the $\bar{x}_i$ points into "Pass" and "Fail" classes, such that the distance between the hyperplane and the closest support vector for each class is maximized. A generic hyperplane can be written as a function of each $\bar{x}_i$ point as:

$$\bar{\omega}^T \bar{x}_i - \gamma = 0 \quad \text{where } \bar{\omega} \text{ is the normal vector to the hyperplane}$$

Now, assuming that the data-set is linearly separable, two parallel hyperplanes are selected such that the distance between them is maximized:

$$\bar{\omega}^T \bar{x}_i - \gamma = 1 \quad \text{which defines the boundary for the class with label "Pass"}$$

$$\bar{\omega}^T \bar{x}_i - \gamma = -1 \quad \text{which defines the boundary for the class with label "Fail"}$$

However, in order to prevent that the data points can fall into the margin, the following constraint (hard margin) is added for each data sample:

$$\bar{\omega}^T \bar{x}_i - \gamma \geqslant 1 \quad \text{if } \bar{y}_i = \text{“Pass”} \quad \text{for } i = 1, 2, \ldots m$$

$$\bar{\omega}^T \bar{x}_i - \gamma \leqslant 1 \quad \text{if } \bar{y}_i = \text{“Fail”} \quad \text{for } i = 1, 2, \ldots m$$

This constraint can be rewritten as

$$\bar{y}_i \, (\bar{\omega}^T \bar{x}_i - \gamma \geqslant 1) \text{ for } i = 1, 2, \ldots m.$$

The distance between those two hyperplane defines the margin and is given by $\frac{2}{\|\bar{\omega}\|}$, which means that in order to maximize the margin, the $\|\bar{\omega}\|$ has to be minimized. Therefore, the final optimization problem can be formulated as:

$$\text{Minimize } \|\bar{\omega}\| \text{ subject to the constraint } \bar{y}_i \, (\bar{\omega}^T \bar{x}_i - \gamma \geqslant 1) \text{ for } i = 1, 2, \ldots m$$

Finally, the optimal classifier is determined by the $\bar{\omega}$ and γ that solve this problem, while the hyperplanes boundary is defined by the $\bar{x}_i$ which is located closest to it.

5.3.2 Model performance evaluation metrics

The performance of a classification model is typically assessed by looking at its accuracy, which is computed as the ratio of correct predictions divided by all predictions and is typically reported in percentage. Another metric is the misclassification error (MCE) which refers to the ratio of wrong predictions divided by the total number of predictions. However, those metrics are typically not sufficient to assess the effectiveness of a predictive model, especially in the presence of imbalanced data-set, where the classification accuracy may be misleading. A model trained on a data-set with large class imbalance may have high classification accuracy only because the model can predict the value of the majority class for all the predictions; this is also known as “Accuracy Paradox”.

A more reliable method to assess the prediction performance of a classifier is the confusion matrix, reported in Figure 5.4 (a) for a binary classification problem, in which the outcomes are labeled as “Positive” (P) or “Negative” (N).

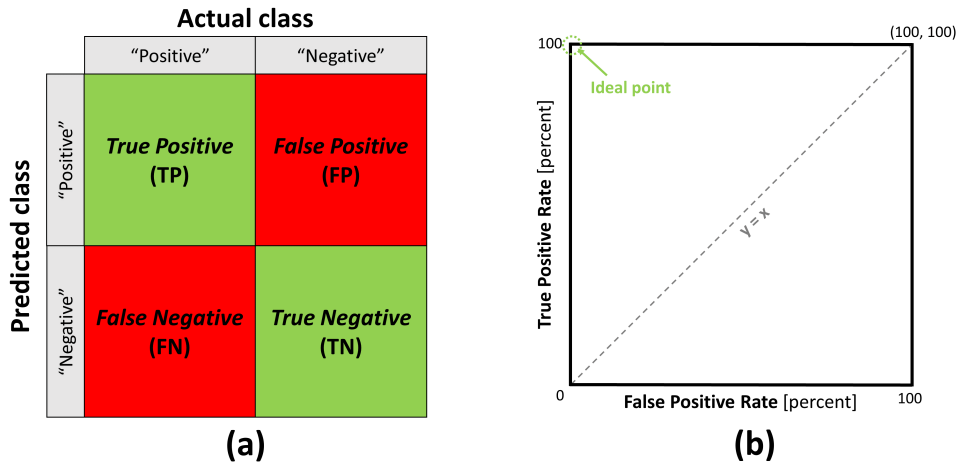

Figure 5.4 Illustration of (a) the confusion matrix for a binary classification problem and (b) the receiver operating characteristic (ROC) curve.

Therefore, there are four possible outcomes and the table consists of two rows and two columns, representing the "Actual class" in the data-set and the "Predicted class" by the model, respectively. In particular, the number of True Negatives (TN) is the number of negative samples correctly classified, the number of False Positives (FP) is the number of negative samples incorrectly classified as positive, the number of False Negatives (FN) is the number of positive samples incorrectly classified as negative and finally, the number of True Positives (TP) is the number of positive samples correctly classified. From the confusion matrix it is possible to derive different metrics:

- *Precision or Positive Predictive Value (PPV)*, which is given by the ratio of the True Positives and the sum of True Positives and False Positives. Therefore, a low value indicates many False Positives.

- *Negative Predictive Value (NPV)*, which is given by the ratio of the True Negatives and the sum of True Negatives and False Negatives. Therefore, a low value indicates many False Negatives.

- Recall or Sensitivity or True Positive Rate (TPR), which is given by the ratio of the True Positives and the sum of True Positives and False Negatives.

Therefore, a low value indicates many False Negatives, while a value of 1 means that all actual positives are correctly identified as such.

- *Specificity or True Negative Rate (TNR)*, which is given by the ratio of the True Negatives and the sum of True Negatives and False Positives. Therefore, a low value indicates many False Negatives, while a value of 1 means that all actual negatives are correctly identified as such.

- *False Positive Rate (FPR)*, which is given by the ratio of the False Positives and the sum of False Positives and True Negatives.

- *False Negative Rate (FNR)*, which is given by the ratio of the False Negatives and the sum of False Negatives and True Positives.

- *Balanced accuracy*, which is given by normalizing the true positive and the true negative predictions by the number of positive and negative samples, respectively, and dividing their sum by two. In practice, it expresses the mean value of the Sensitivity and the Specificity.

- *F1 score or F Score or F Measure*, which is given by two times the product of the Precision and the Recall, divided by its sum. In practice, it expresses the balance between the Precision and the Recall (i.e. reaches its best value at 1, which means perfect precision and recall and worst value at 0).

Furthermore, in the presence of a high class imbalance with unequal error costs, it is more effective to use of the Receiver Operating Characteristic (ROC) curve, which is a standard technique to express the classifier performance by varying its discrimination threshold [97]. The ROC space, illustrated in Figure 5.4 (b), is created by plotting the percentage of FPR (reported on the x-axis) against the percentage of TPR (reported on the y-axis) as a function of some classifier parameters. Essentially it expresses the trade-offs between the True Positives (i.e. benefits) and False positives (i.e. costs). In particular, the line $y = x$, which divides the ROC space, represents a random guess of the class, therefore the point above and below that line represent good and bad prediction performance, respectively. The ideal point on the ROC curve (i.e. representing the best prediction model) would be found in the upper

left corner or (0,100), which means that no False Negatives and no False Positives samples are predicted by the model. The area under the curve (AUC) is a useful performance metric for a ROC curve because it is independent of the decision criterion [98]. Extending the ROC curves for multi-class classification problems turns out to be impractical due to increase ROC space dimensions [99]. An approach for the particular case with three classes is proposed in [100]. Furthermore, the ROC curve has been extended to regression problems, defining a regression error characteristic (REC) [101] and a regression ROC curve (RROC) [102].

5.3.3 Model validation methods

Estimating the performance of a model, only based on the predicted values from the training set and the original response, would only validate the model on the data used for training. However, the trained model needs to ensure good generalization performance on unseen data (i.e. data not used for training the model), therefore it is essential to validate the stability of a machine learning model. The simplest validation method is the holdout method, which consists in splitting the original data-set into a training set and a test set used to evaluate the performance of the model. This method doesn´t introduce any additional computational effort, but the model performance estimation may suffer from high variance because of the randomness in selecting the data-set used for training and testing purpose. Furthermore, removing data samples which can be potentially used for training (i.e. the one included in the test set) may result in under-fitting or losing important information contained in the original data-set.

Cross validation is a method that provides a more effective performance assessment of a machine learning model by combining (i.e. averaging) the results over multiple subsets of the original data-set, which are divided into training and test set [103]. This method is used to assess the prediction performance of a model on unseen data (i.e. generalization performance), avoiding model selection bias or over-fitting problems [104]. In general, the validation techniques can be divided in *exhaustive* and *non-exhaustive cross validation methods*. The first ones compute all possible combinations of splitting the data into training set and test sets:

- *Leave-$\mathscr{P}$-Out Cross Validation*, which consists of removing p data points from the training data to be used as the validation set and repeating it for all the possible combinations. Then the error is the average of all combinations. However, for a higher value of p, this approach may become infeasible.

- *Leave-One-Out Cross Validation*, which is a particular case of the previously described method (i.e. $p = 1$). This limits the number of possible combinations to the number of points in the original data-set, reducing the computation time.

Instead, the *non-exhaustive cross validation methods* consider only a fixed number of subsets, such as:

- *$\mathscr{K}$-fold cross-validation*, which consists of repeating the holdout method k times (i.e. data are divided in k subsets). Then, one of the k subsets per time is used as a validation set, while the other k-1 subsets constitute the training set. Therefore, most of the data are used for training and validation, resulting in a more effective assessment of the model performance. In particular, the error is estimated as the average over all k combinations, reducing bias issue and variance. In general, k=5 or 10 is a common approach.

- *Stratified k-fold validation*, which is a variation of the k-fold validation in order to deal with imbalanced data-sets. In practice, in case of a classification problem, this technique ensures that the same percentage of data which belong to a certain target class is contained in each fold, while for a regression problem, it ensures that the mean of the target value is the same in each fold.

Chapter 6

A SoC-package co-design methodology based on SVM models

Considering the increasing complexity of the SoC-package design for next generation of automotive products, a conventional chip-package co-design approach, where IP block models and package model are combined together in a system-level test-bench, may result in running complex and time-consuming system-level simulations that may slow down the overall development cycle. This is amplified by the huge number of derivative package designs which are typically developed for each SoC generation (more than 10 different versions).

In this chapter a machine learning approach is investigated in order to avoid tedious and time consuming system-level simulations and to minimize the number of frequency points to be extracted via EM-filed solver for package modeling. In particular, a sequential feature selection algorithm is used to identify the optimal number of features from the circuit simulation data at chip-level and the EM-field simulation data at package-level to train a support vector machine (SVM) model to predict the ADC RMS-noise behavior. Results are compared against post-silicon measured data, proving the effectiveness of this approach in comparison to a conventional chip-package co-design as it has been performed up to now.

6.1 Problem formulation overview and available data-set

An overview of the main SoC-package development trend, along with the main challenges and risks, associated to next generation of automotive SoC-package design, is reported in Figure 6.1.

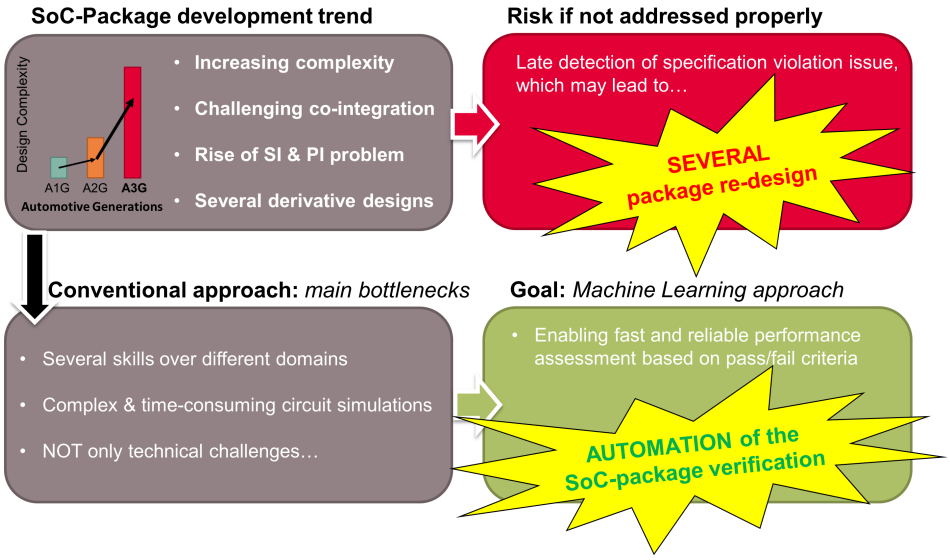

Figure 6.1 Overview of an automotive SoC-package development.

A conventional chip-package co-design methodology, as the one presented in previous chapters, would require several iterations for:

- *Aggressor-Victim IP blocks model simplification*, to be performed each time a concept or topology change is implemented (manual work).
- *Package-Board interconnect model extraction*, to be performed each time a layout change occurs (time consuming).
- *System-level simulation test bench*, which may suffer from convergence issue due to the integration of the package-board model into a circuit simulator (passivity, causality of the S-parameter model).

This highlights how knowledge from multiple domains is required to cope with a typical chip-package-board co-design challenge. While, for an ML-based co-design

approach, the quality of the data-set is the main contributor to achieve the desired learning performance.

6.1.1 Test case description and available data

The test case investigated in previous chapters (i.e. the coupling between the DC/DC converter and ADC analog inputs) is reused in this chapter. The available data-set, reported in Figure 6.2, consists of the RMS-noise measurements data from 4 package designs with about 60 to 100 analog input channels each. The RMS-noise performance prediction problem is formulated as a binary classification problem ("Pass/Fail" criteria) and addressed via SVM model. In addition, a multi-level classification problem ("level-0/1/2" criteria) is formulated and addressed, using an error-correcting output codes (ECOC) classifier model, where the classifier consists of multiple binary SVMs.

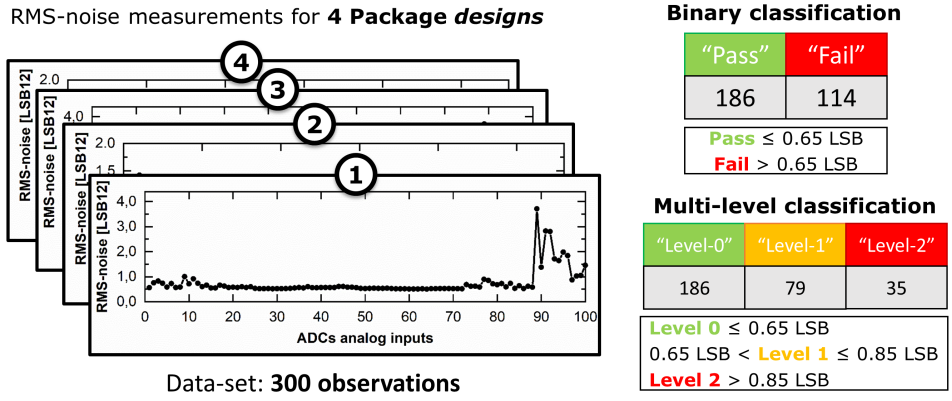

Figure 6.2 Overview of the binary and multi-level classification problem.

It can be noted that class imbalance starts to arise as the number of classes increases from two to three. This issue is addressed by using the chip-package co-design methodology developed in chapter III to artificially create additional RMS-noise simulation-data from different package designs in order to populate the classes equally.

6.2 SVM-based SoC-package co-design methodology

The SVM models have been developed by means of the machine learning toolbox available in MATLAB [105]. The output of the model is the prediction of the RMS-noise level from the S-parameters of a package design. In particular, only a subset of S-parameters frequency points (referred as features in the following discussion) which are relevant for the output prediction is used. The main steps sketched in Figure 6.3 can be summarized as follows:

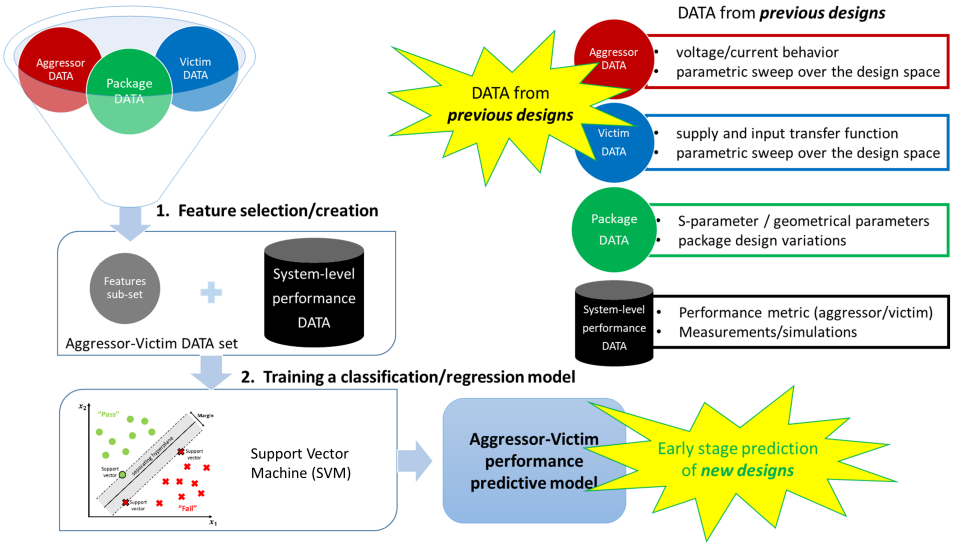

Figure 6.3 Overview of the machine learning steps and data-set.

- *Data-set formatting*
  First, the S-parameter data are divided into discrete levels to improve the filtering performance of the chosen feature selection method. Then, a 20% holdout is applied to build the test-set.

- *Feature Filtering*
  As a feature pre-processing step, a fast correlation-based filter method [83] is used to cope with the high correlation amongst the S-parameters elements. In particular, the feature selection toolbox (FEAST) [106] for MATLAB is used to select the most relevant feature for the output prediction.

- *Sequential Feature Selection*
  A forward sequential feature selection algorithm is used in a wrapper manner, considering the misclassification error (MCE) of the chosen learning algorithm (SVM with Gaussian Kernel) as performance metric to evaluate each subset of features towards the identification of the optimal subset which corresponds to the minimum MCE for the SVM model.

- *SVM model training and validation*
  An SVM classification model with a Gaussian kernel is chosen to describe the non-linear behavior of the coupling mechanism in a better way and trained using a 10-fold cross-validation for the assessment of the prediction performance.

6.2.1 Validation results and main advantages

The SVM models are further validated against the measurements data of an additional package design, not considered in the original data-set. As reported in Figure 6.4, a good classification performance is achieved for both binary and multi-level problems.

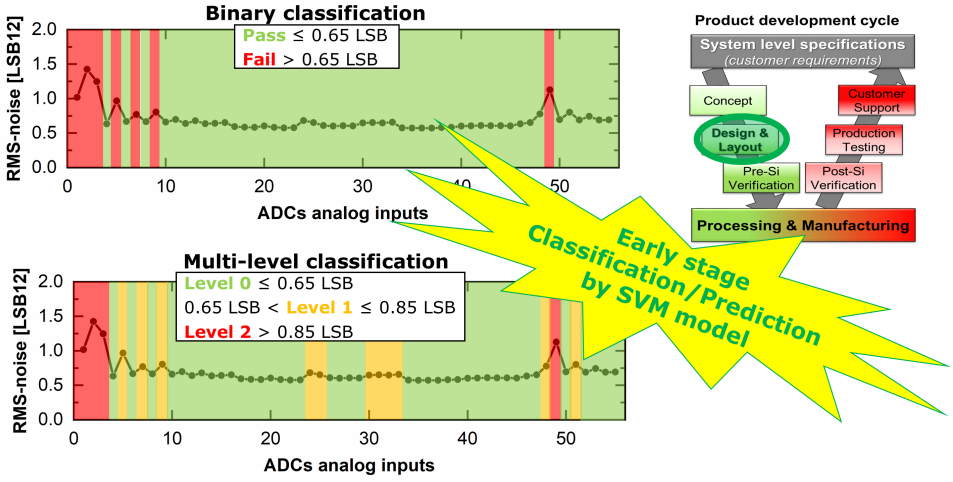

Figure 6.4 Validation results for binary and multi-level classification problems.

Such an approach allows to deal with the high number of package design derivatives, which are typically developed for each automotive AMS SoC generation. The main advantages can be summarized as follows:

- Quick assessment of the package design performance
- Limited number of frequency points to be extracted via EM-field solver
- Avoid complex system-level time domain simulations

Furthermore, as reported in Figure 6.5, a significant speed up is achieved compared to a conventional chip-package co-design approach.

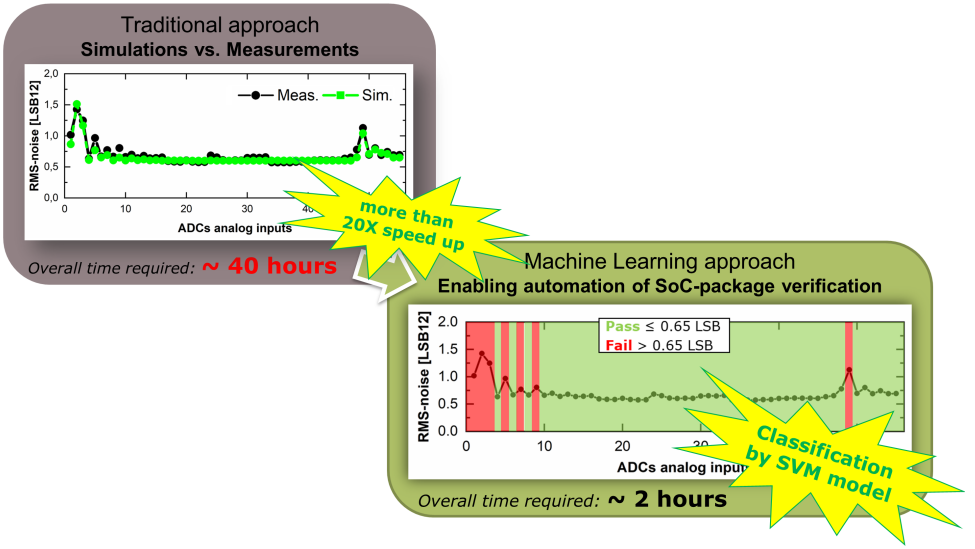

Figure 6.5 SVM-based and conventional co-design approach comparison.

This significant improvement mainly arises from the limited number of frequency point that need to be extracted via EM-field solver (avoiding to compute the DC point) in an ML-based approach compared to a conventional chip-package co-design approach, where several points (including the DC point) need to be extracted to guarantee the stability of a system-level time domain simulation.

6.3 Future perspective on ML-based chip-package-board co-design

As reviewed in chapter V, a machine learning approach exploiting ANNs and SVMs, has been proven to be a valid option in behavioral modeling of a variety of electronic circuits and systems, ranging from basic and complex analog block up to high-speed interface systems in order to enable faster design space exploration for design optimization. Therefore, it is reasonable to assume that the SVM-based co-design methodology developed here for the test case involving a sensitive ADC (acting as a victim) and a DC/DC converter module (acting as the aggressor) can be extended to cover any aggressor-victim pairs within a complex SoC-package design system. A sketch of a potential ML-based co-design framework for aggressor-victim identification is reported in Figure 6.6.

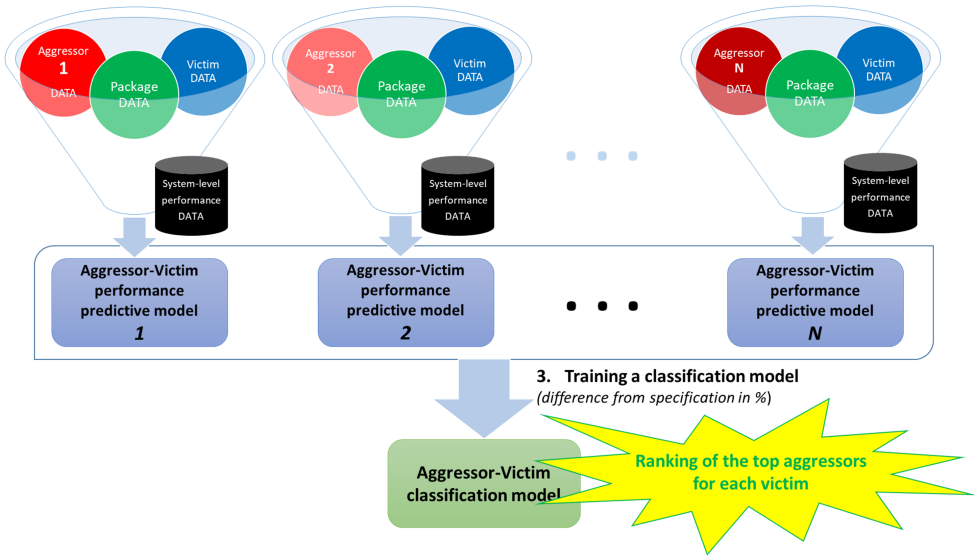

Figure 6.6 Overview of the aggressor-victim pairs classification framework.

For example, a direct application of the developed SVM-based modeling approach to predict potential coupling issue at package-level from or to an high-speed interface (HSI) design (i.e. either via signal path or power supply path), may lead to the following main challenges:

- *Achievable accuracy of the prediction model*
  Compared to the investigated test case (i.e. DC/DC converter impact on ADC analog inputs), where a pass/fail criteria (binary classification problem) or a discretization in few levels (multi-level classification problem) can be sufficient as the output prediction target, an output prediction target within few mV accuracy would be needed for the HSI case. The prediction accuracy (required granularity in terms of mV) will definitely impact the size of the data-set (i.e. the number of observations required for each class to avoid imbalanced data and accurately predict the output), therefore more test cases would be needed to train the SVM classification model in order to achieve the required prediction performance.

- *Imbalanced Data-set issues*
  Compared to the investigated test case (i.e. DC/DC converter impact on ADC analog inputs), where different analog channel variants (up to 100) are available in each package design, for an HSI only few digital channels would be available depending on the number of transmitter/receiver channels required by the application. This would require a strategy to virtually build a wider variation package design space to be used for system-level simulations in order to create a balanced data-set for accurate performance prediction.

As a further development direction, one may think to consider the full chip-package-board interconnect path, to take into account also the variations in chip and board physical design implementations. Such a prediction problem would encounter the following challenges:

- *Data-set creation*
  As for the previous challenge, also in this case a strategy how to artificially build different cases for both the chip and board interconnects is required.

- *Increasing complexity*
  Extending the approach to include more of the chip and board interconnects would definitely lead to an increased complexity, therefore a strategy how to cope with it needs to be figured out. The extension to the chip interconnect

design is expected to present the main challenge due to the higher complexity compared to the board interconnects design.

The common point in both the examples discussed before, is the fact that having a lot of measured observations, as for the DC/DC vs. ADC case, would be not feasible in practice. Therefore it is clear that the enabling step for a machine learning-based approach would be a reliable system-level simulation setup, validated against a reference measurement. This would enable the generation of the required data-set by running system-level simulations for the virtually created chip-package-board interconnects variants.

Therefore, considering a scenario where the performance of all the potential aggressor-victim pairs can be accurately predicted by an ML-based approach, an additional classifier would enable the ranking of the worst case aggressor-victim pair in order to focus only on the critical pairs for each package design derivative. Such a framework could be enhanced to solve the SoC-package floorplan optimization problem by investigating the achievable accuracy in predicting the aggressor-victim performance at system-level using the available data during chip-package physical design floorplan. As sketched in Figure 6.7, these informations include the IP blocks position, pin assignments on the die pad-frame and ball assignments on the board-side. In addition, also the information about the aggressor-victim interconnects can be considered from previous package designs and for a given package technology (e.g. distance and parallel length between interconnects).

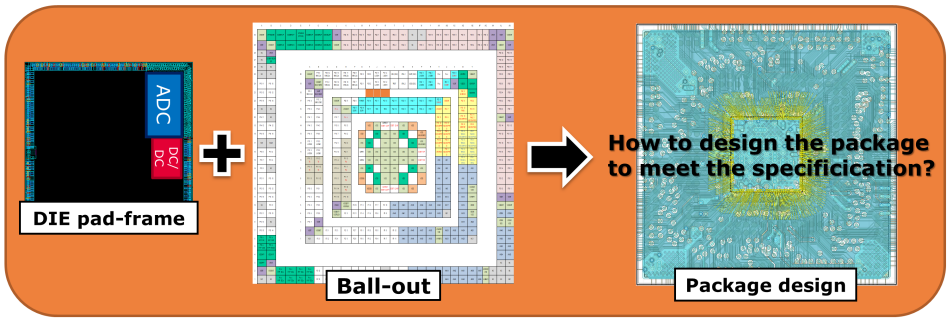

Figure 6.7 Overview of the SoC-package floorplan optimization problem.

Solving this optimization problem would allow to assess the package performance already in the early stage of the design cycle, when the package design is still not available, leading to faster ECOs loop during the development cycle, which in turn results in reduced development cost and time-to-market.

6.4 Conclusions

Although early stage co-design methodology, to assess and optimize the SI and PI of a complex chip-package-board system, is well established for high-speed digital circuit design (e.g. employing IBIS models to run faster and efficient transient simulation), the same is not available yet for complex analog/mixed-signal blocks. In such a case, using full transistor-level model for system-level co-analysis and co-simulation, would not be feasible due to the prohibitive transient simulation time. Simplified models need to be created manually, which require a deep understanding of the block functionality in order to achieve a good trade-off between model accuracy and simulation time.

This work addressed the co-integration of a key mixed-signal block such as the ADC in a complex automotive SoC-package design system. In particular, as an aggressor-victim pair application example, the impact of the coupling between the DC/DC converter on the ADC performance has been investigated, considering the RMS-noise of the ADC analog input channels as a performance metric. Two main aspect of the AMS SoC-package development have been addressed:

- *SoC-package design complexity*
- *High volume of package design derivatives for each SoC generation*

In order to deal with the design complexity, a SoC-package co-simulation methodology exploiting a modeling approach at different-levels of abstraction has been developed to predict the system-level RMS-noise performance of the ADC analog inputs. Based on the developed co-simulation methodology, which has also been validated against measurements data, a step-by-step SoC-package co-design methodology has been proposed to guide the package design development by identifying the exact locations that need to be optimized to meet the system-level specifications.

Simulation results compared with post-silicon RMS-noise measurements data for different package design and re-design have proven the effectiveness of the proposed approach in optimizing the SoC-package system design.

However, the high volume of package design derivatives, which need to be developed for each SoC generation, requires a higher level of automation to achieve a fast and reliable early stage assessment of the SoC-package performance. Therefore, an SVM-based SoC-package co-design methodology has been proposed to avoid tedious and time consuming system-level simulations and minimize the number of frequency points to be extracted via EM-filed solver for package modeling. With such an approach package designers can confidently assess the performance of the package design for a generic aggressor-victim pair achieving a faster sign-off based on the pass/fail criteria defined at system-level. Chip designers may also benefit from it by performing design space exploration during the early stage of the SoC-package development.

Finally, research directions have been indicated to further develop an ML-based co-design framework to address SI/PI challenges amongst all potential aggressor-victim pairs in the early stage of the development cycle, which is essential to achieve "right first time" solutions even under the ever growing pressure to save costs and time-to-market.

List of Publications

1. **Title:** "Understanding the Potential and Limitations of Tunnel-FETs for Low-Voltage Analog/Mixed-Signal Circuits"
   Authors: *F. Settino, M. Lanuzza, S. Strangio, F. Crupi, P. Palestri, D. Esseni, and L. Selmi*
   (**Published on IEEE Transactions on Electron Devices Journal, 2017**)

2. **Title:** "A virtual III-V Tunnel FET technology platform for ultra-low voltage comparators and level shifters"
   Authors: *F. Settino, M. Lanuzza, S. Strangio, F. Crupi, P. Palestri, and D. Esseni*
   (**Oral Presentation at 13th Conference on Ph.D. Research in Microelectronics and Electronics, PRIME 2017**)

3. **Title:** "Simulations and comparisons of basic analog and digital circuit blocks employing Tunnel FETs and conventional FinFETs"
   Authors: *F. Settino, S. Strangio, M. Lanuzza, F. Crupi, P. Palestri, and D. Esseni*
   (**Poster presentation at 5th Berkeley Symposium on Energy Efficient Electronic Systems** & **Steep Transistors Workshop, E3S 2017**)

4. **Title:** "Digital and analog TFET circuits: design and benchmark"
   Authors: *S. Strangio, F. Settino, P.Palestri, F. Crupi, P. Palestri, D. Esseni, and L. Selmi*
   (**Published on Solid-State Electronics Journal, 2018**)

5. **Title:** "Chip/Package/Board Co-Simulation Methodology for Crosstalk between DC/DC Converter and ADC Input Channels"

Authors: *F. Settino, T. Brandtner, V. Subotskaya, A. Levanto, M. Faricelli, F. Praemassing, L. Della Ricca, H. Koffler, P. Palestri, and F. Crupi*
(**Oral presentation at IEEE 7th Electronics System-Integration Technology Conference, ESTC 2018**)

6. **Title:** "Embedded Power Management for Automotive Microcontroller Units (MCUs) and its Challenges"
Authors: *F. Praemassing, R. Priewasser, F. Settino, G. Perini, W. Hoellinger, R. Riederer, D. Hesidenz, and B. Mathews*
(**Invited presentation at Integrated Power Conversion and Power Management, PrSoC 2018**)

7. **Title:** "Package Design Methodology for Crosstalk Mitigation between DC/DC Converter and ADC Analog Inputs in Complex SoC"
Authors: *F. Settino, T. Brandtner, J. Niederl, F. Praemassing, H. Koffler, P. Palestri, and F. Crupi*
(**Oral presentation at IEEE 23rd Workshop on Signal and Power Integrity, SPI 2019**)

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